Software Packet Processing and Hardware Packet Processing

— Architecture —

JANOG 37 @ Nagoya

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## Self introduction: Kentaro Ebisawa

### Network related

**Selection and Deployment Support of international NW products**
- IPsec, ADSL, L2TP, ATM, MPLS (focused on Edge)
  - @Netmarks

**Engineer & Manager @ Support Center**
- Content delivery & storage @NetApp

**Design/development of network equipment**
- IPv6v4 Gateway (ASIC) @Sable Networks
- OpenFlow switch (FPGA) @Riava Networks
- Network OS @Ponto Networks

### Others

**SaaS development**
- @SGI / MEX

**Design and Build support for OSS/BSS**
- Solution Architect @Parallels
  - SaaS/IaaS launch assistance at Asian telecom carrier

### Community

- Vyatta Users Group (former)
- Lagopus Users Group
- OpenVZ (Virtuozzo)
Today’s talk

1. Router (L3 switch) Architecture Overview

2. About Packet Processing

3. Differences between Hardware (ASIC) and Software (CPU) (focused on Architecture)

...differences between hardware and software by Nakajima (details)...

advantages & disadvantages; bottleneck comparison
Function Block of Router (Layer 3 switch)

- Management/policy-plane
  - CLI / Configuration/ NETCONF
- C-plane
  - BGPd
- OSPFd
- Routing daemon
- Routing table (RIB)
- Forwarding table (FIB)
- Packet processing
- D-plane
- Adjacent routers
The general architecture of a router (Layer 3 switch)

• **Management-plane (M-plane)**  
  - Sets the interfaces, address, and routing protocols  
    - CLI, NETCONF, RESTCONF  
  - Provides operational status for monitoring  
    - SNMP, syslog

• **Control-plane (C-plane)**  
  - Looks up adjacent nodes and network topology  
  - Processes routing protocols  
    - BGP, OSPF, ISIS  
  - Updates and Manages Routing Information Base (RIB) / Forwarding Information Base (FIB), based on routing information

• **Data-plane (D-plane)**  
  - Forwards and Processes the transit traffic (packets) based on FIB
Type of packet to be processed (1) | Transit traffic (packets)

Adjacent routers

<table>
<thead>
<tr>
<th>C-plane</th>
<th>BGPd</th>
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</thead>
</table>

Routers, Layer 3 switches

<table>
<thead>
<tr>
<th>Management/policy-plane</th>
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</thead>
<tbody>
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<td>CLI / Configuration / NETCONF</td>
</tr>
</tbody>
</table>

| C-plane | BGPd |

| OSPFd |

Routing daemon

| Routing table (RIB) |

D-plane

| Forwarding table (FIB) |

| Packet processing |

Adjacent routers

| C-plane | BGPd |

| D-plane |

Transit traffic

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Type of packet to be processed (2) | Route Exchange with adjacent nodes via BGP

- **Adjacent routers**
  - C-plane
    - BGPd
  - D-plane
- **Routers, Layer 3 switches**
  - Management/policy-plane
    - CLI / Configuration/ NETCONF
  - Routing daemon
  - Routing table (RIB)
  - Forwarding table (FIB)
  - Packet processing
- **Adjacent routers**
  - C-plane
    - BGPd
  - D-plane

Logical connections: D-plane to C-plane via BGPd; C-plane to D-plane via BGPd.
What’s the difference between hardware implementation and software implementation?

- Besides the difference in D-plane implementation, they have nearly the same construct.
- The difference is whether “dedicated hardware or ASIC” is used for high-speed packet processing (Fast Pass), or all are implemented by “software”.

### Table: Hardware vs. Software Implementation

<table>
<thead>
<tr>
<th>Type</th>
<th>Hardware Implementation</th>
<th>Software Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>M-plane</td>
<td>Implementation: software on CPU controlling switch</td>
<td>Implementation: software on CPU</td>
</tr>
<tr>
<td></td>
<td>OS: Linux/BSD</td>
<td>OS: Linux/BSD</td>
</tr>
<tr>
<td>C-plane</td>
<td>Implementation: software on CPU controlling switch</td>
<td>Implementation: software on CPU</td>
</tr>
<tr>
<td></td>
<td>OS: Linux/BSD</td>
<td>OS: Linux/BSD</td>
</tr>
<tr>
<td>D-plane</td>
<td>Implementation: packet processing implemented on ASIC or FPGA</td>
<td>Implementation: software on CPU</td>
</tr>
<tr>
<td></td>
<td>as fixed circuit</td>
<td>Packet I/O: via NIC (PCIe)</td>
</tr>
<tr>
<td></td>
<td>Packet I/O: dedicated circuit</td>
<td>OS: Linux/BSD</td>
</tr>
</tbody>
</table>

### Diagram:

- **Routers and Layer 3 switches**
  - Management/policy-plane
    - CLI / Configuration/ NETCONF
  - C-plane
    - BGPd
    - OSPFd
    - Routing daemon
    - Routing table (RIB)
  - D-plane
    - Forwarding table (FIB)
    - Packet processing
D-plane basic processing

**Software implementation**

Software implementation of packet processing through OS NW stack

CPU

Network stack

Memory

NIC

Phy

Signaling, C-plane msg

Transit-traffic

**Modern software implementation of packet processing**

CPU

Network stack

Memory

NIC

Phy

Signaling, C-plane msg

Transit-traffic

**Hardware implementation**

Hardware implementation of packet processing

CPU for Hardware Control

Network stack

Memory

PCI-Exp

HW fast pass

Phy

Signaling, C-plane msg

Transit-traffic
Actual configuration

Hardware implementation
(commercial silicon switch)

Reference: White Box L3 switch

Software implementation
(general purpose PC server)

Reference: Intel
Summary

The biggest difference = How transit packets are processed

• Hardware: Processed on ASIC (dedicated HW)
• Software: Processed on CPU

White-box switches also perform packet processing on dedicated hardware (ASIC) (although it looks like Linux)

Control packets are both processed by CPU
To be continued...

... the differences between hardware and software (details)...
advantages & disadvantages, and bottleneck comparison