

Software Packet Processing and Hardware Packet Processing

— Architecture —

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Self introduction: Kentaro Ebisawa

Network related

Selection and Deployment Support of international NW products

IPsec, ADSL, L2TP, ATM, MPLS (focused on Edge)
@Netmarks

Engineer & Manager @ Support Center

Content delivery & storage @NetApp

Design/development of network equipment

IPv6v4 Gateway (ASIC) @Sable Networks
OpenFlow switch (FPGA) @Riava Networks
Network OS @Ponto Networks

Others

SaaS development @SGI / MEX

Design and Build support for OSS/BSS

Solution Architect @Parallels
SaaS/laaS launch assistance
at Asian telecom carrier

Community

Vyatta Users Group
(former)

Lagopus Users Group
OpenVZ (Virtuozzo)

Today's talk

1. Router (L3 switch) Architecture Overview

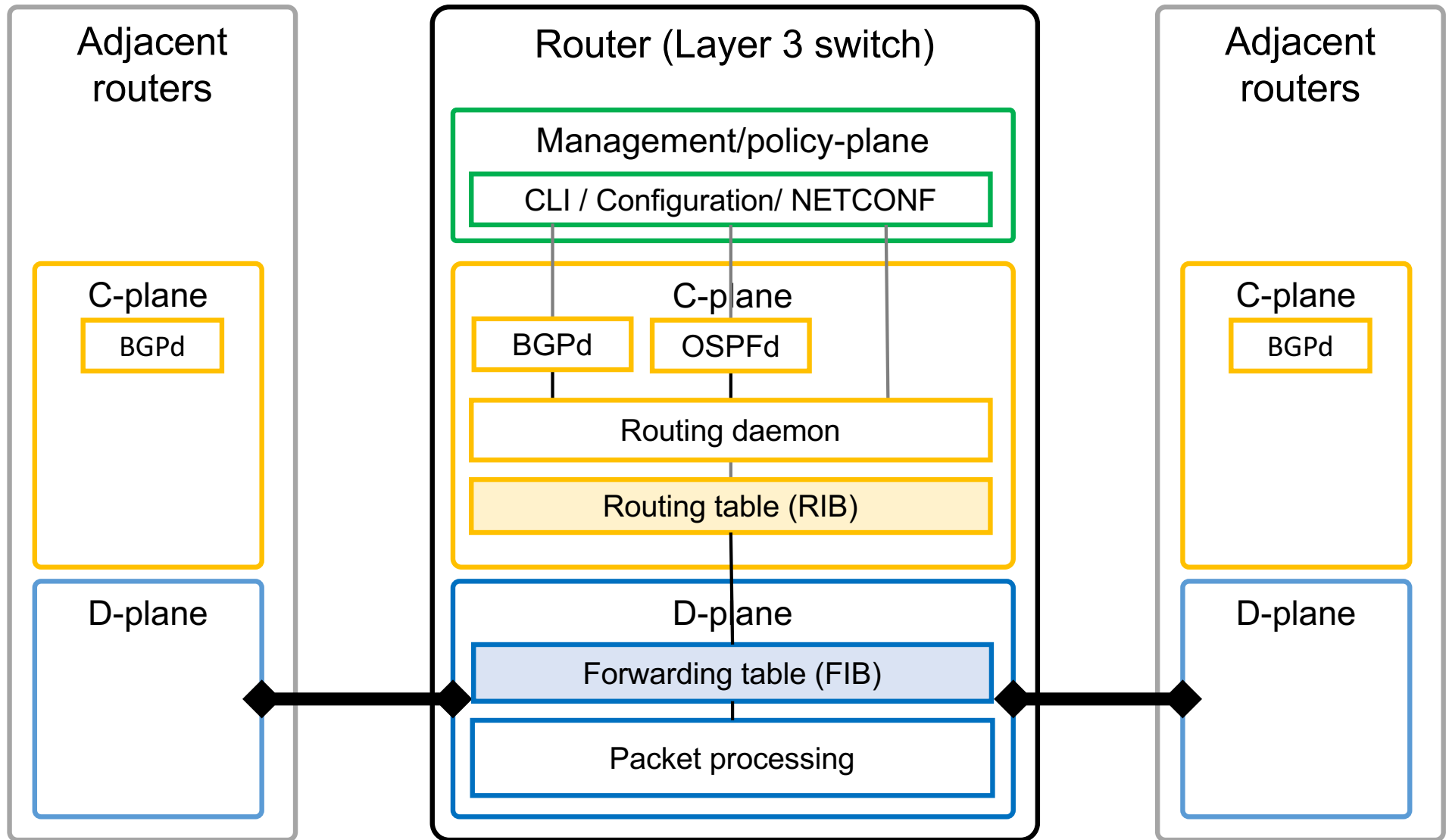
2. About Packet Processing

3. Differences between Hardware (ASIC) and Software (CPU) (focused on Architecture)

...differences between hardware and software
by Nakajima (details)...

advantages & disadvantages; bottleneck comparison

Function Block of Router (Layer 3 switch)



The general architecture of a router (Layer 3 switch)

- Management-plane (M-plane)

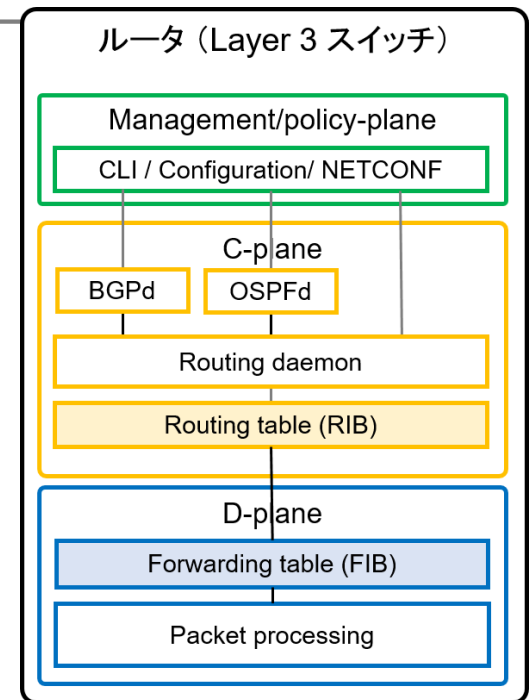
- Sets the interfaces, address, and routing protocols
 - CLI, NETCONF, RESTCONF
- Provides operational status for monitoring
 - SNMP, syslog

- Control-plane (C-plane)

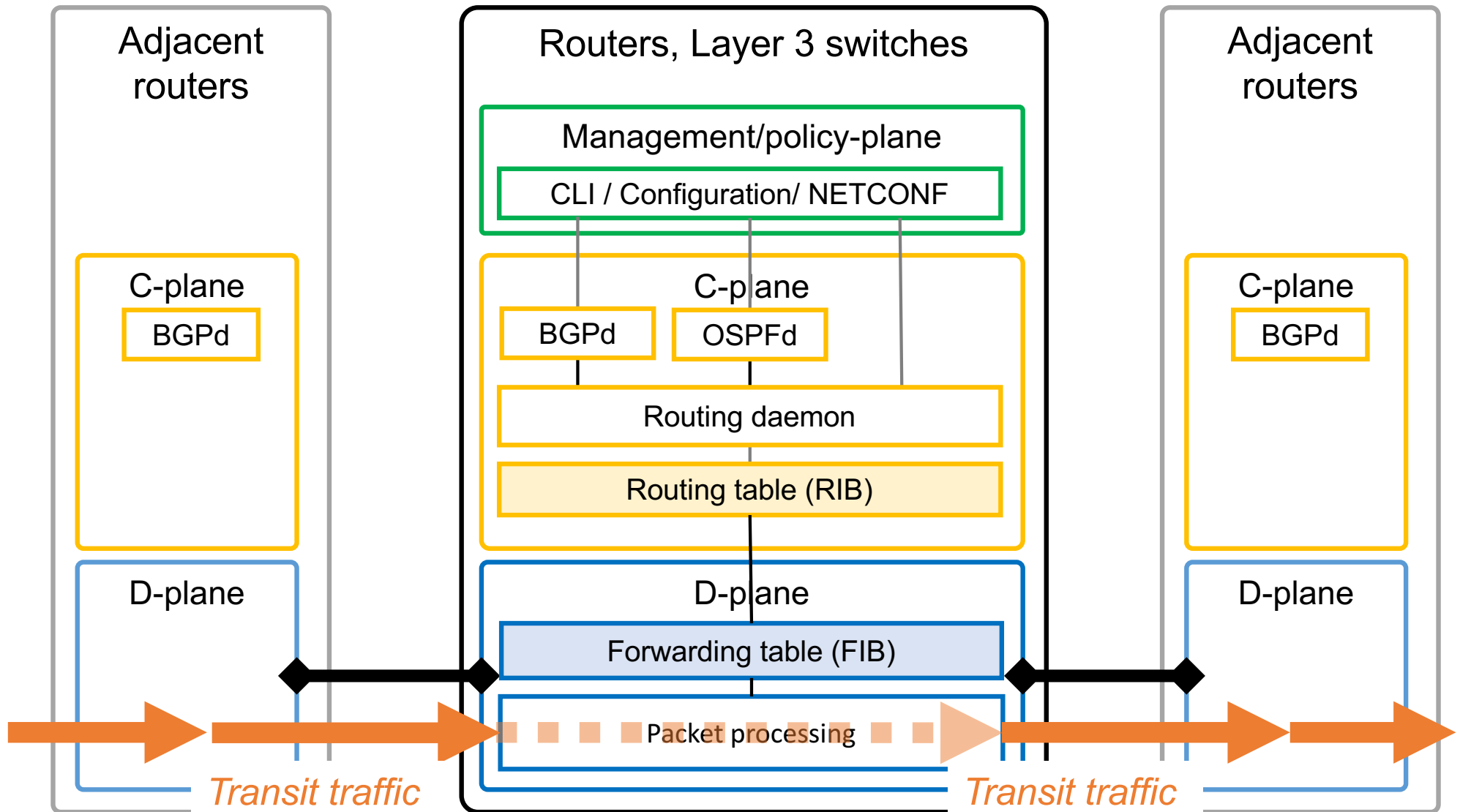
- Looks up adjacent nodes and network topology
Processes routing protocols
 - BGP, OSPF, ISIS
- Updates and Manages Routing Information Base (RIB) / Forwarding Information Base (FIB), based on routing information

- Data-plane (D-plane)

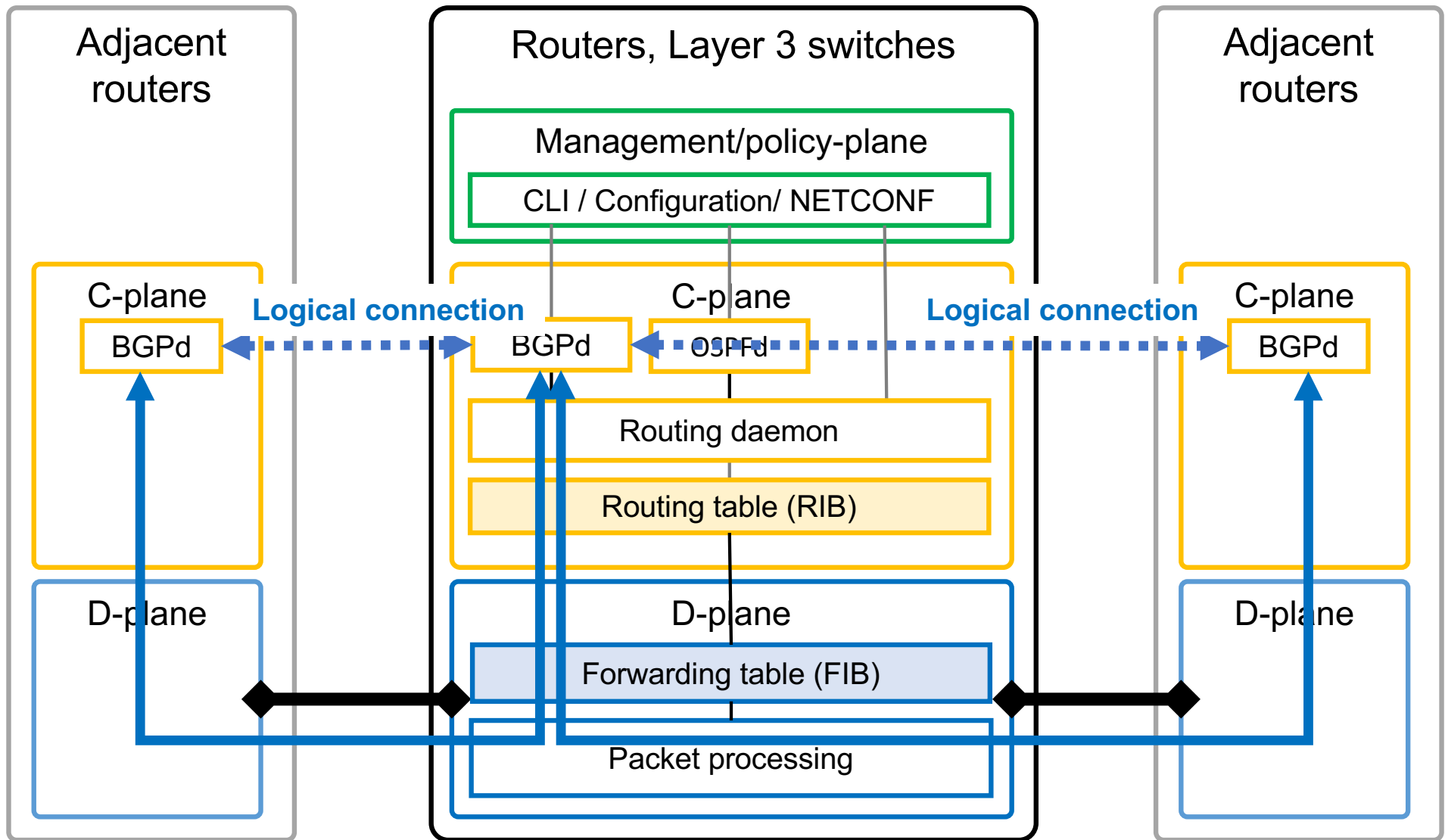
- Forwards and Processes the transit traffic (packets) based on FIB



Type of packet to be processed (1) | Transit traffic (packets)

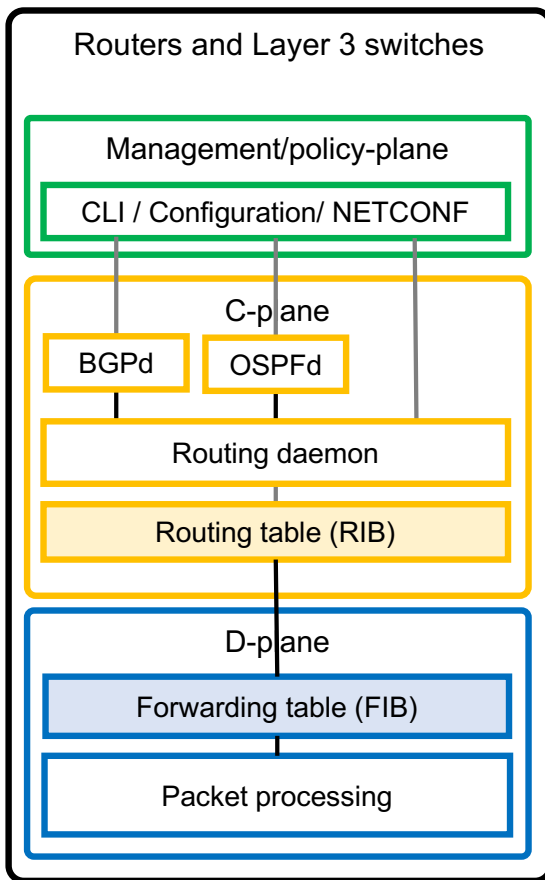


Type of packet to be processed (2) | Route Exchange with adjacent nodes via BGP



What's the difference between hardware implementation and software implementation?

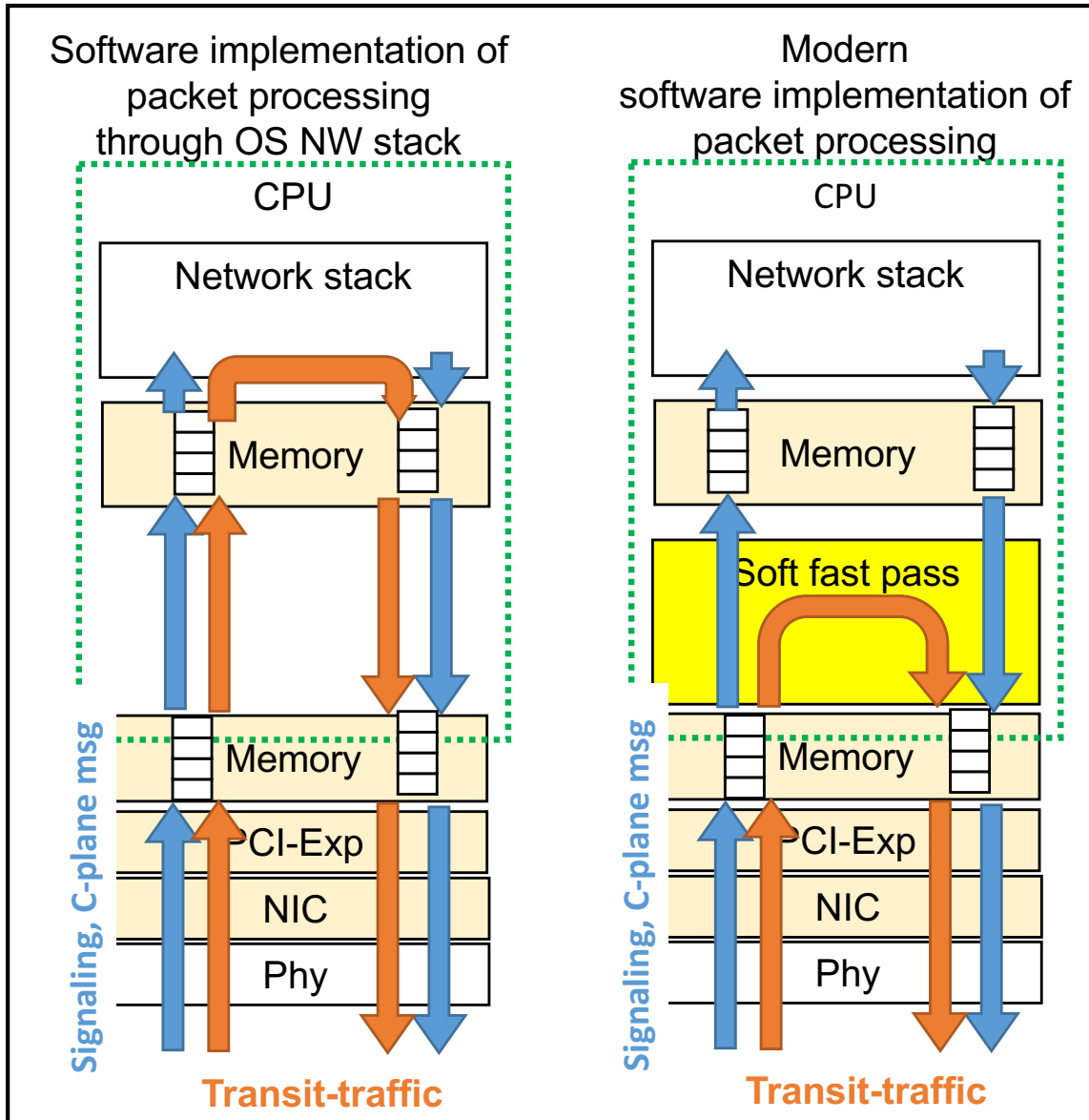
- Besides the difference in D-plane implementation, they have nearly the same construct
- The difference is whether “**dedicated hardware or ASIC**” is used for high-speed packet processing (Fast Pass), or all are implemented by “**software**”.



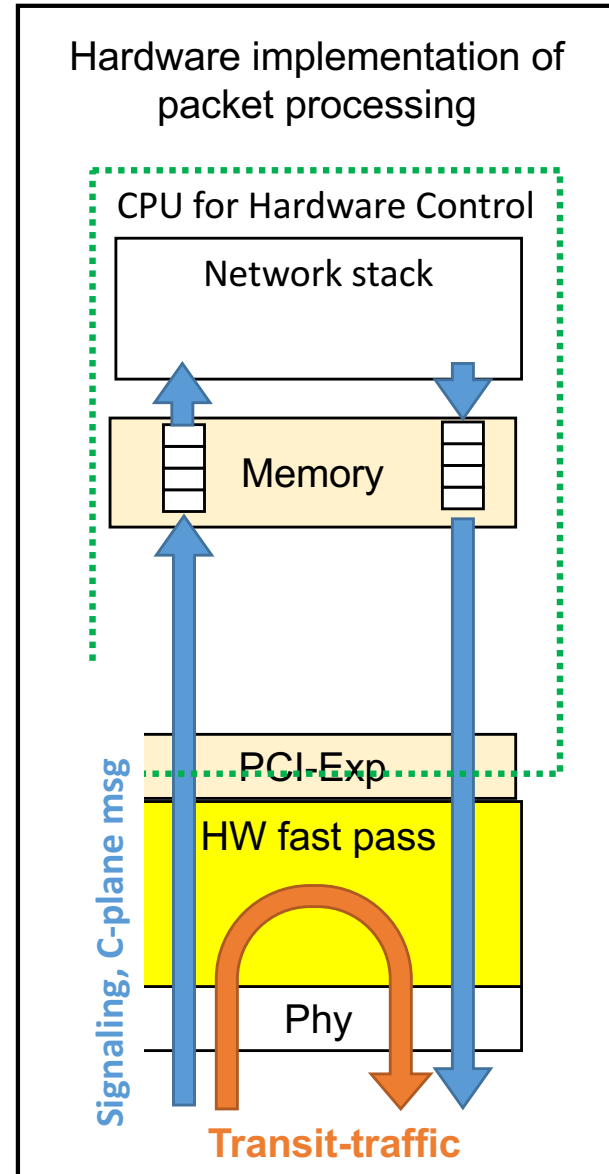
Type	Hardware implementation	Software implementation
M-plane	Implementation: software on CPU controlling switch OS: Linux/BSD	Implementation: software on CPU OS: Linux/BSD
C-plane	Implementation: software on CPU controlling switch OS: Linux/BSD	Implementation: software on CPU OS: Linux/BSD
D-plane	Implementation: packet processing implemented on ASIC or FPGA as fixed circuit Packet I/O: dedicated circuit	Implementation: software on CPU Packet I/O: via NIC (PCIe) OS: Linux/BSD

D-plane basic processing

Software implementation



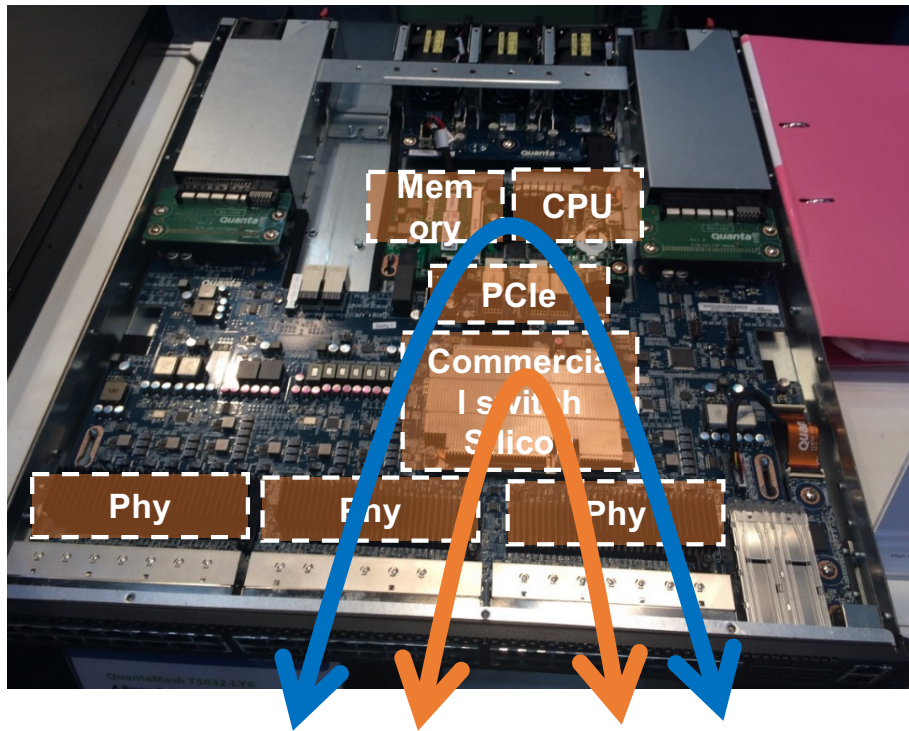
Hardware implementation



Actual configuration

Hardware implementation
(commercial silicon switch)

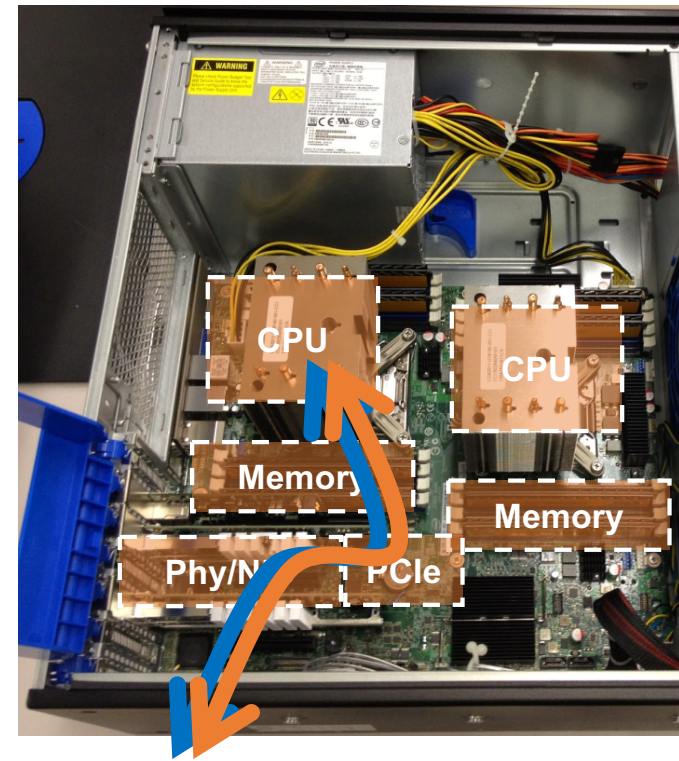
Reference: White Box L3 switch



Signaling, C-plane msg
Transit-traffic

Software implementation
(general purpose PC server)

Reference: Intel



Signaling, C-plane msg
Transit-traffic

Summary

The biggest difference = How transit packets are processed

- Hardware: Processed on ASIC (dedicated HW)
 - Software: Processed on CPU

White-box switches also perform packet processing on dedicated hardware (ASIC) (although it looks like Linux)

Control packets are both processed by CPU

To be continued...

... the differences between hardware and software (details)...
advantages & disadvantages, and bottleneck comparison