

Software packet processing and Hardware packet processing

The advantages and disadvantages

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Self Introduction: Yoshihiro Nakajima

- While at regional university
 - University information education computer management (2000–2005)
 - Research and development of High-performance computing and distributed processing middleware (2003–2008)
- NTT Network Innovation Laboratories
 - Operation of experimental networks (AS173, AS2511) (2008–present)
 - Research and development of IP network transmitter of high-definition video (2008–2011)
 - Research and development of software switch “Lagopus” (2012–present)

Prerequisite knowledge

Modern
software implementation
packet processing
CPU

Network stack

Memory

Soft fast pass

Memory

PCI-Exp

NIC

Phy

100 Gbps /
memory
channel

100 Gbps /
memory
channel

80 Gbps

Signaling, C-plane msg

Transit-traffic

Hardware implementation
packet processing

CPU for Hardware Control

Network stack

Memory

PCI-Exp

HW fast pass

Phy

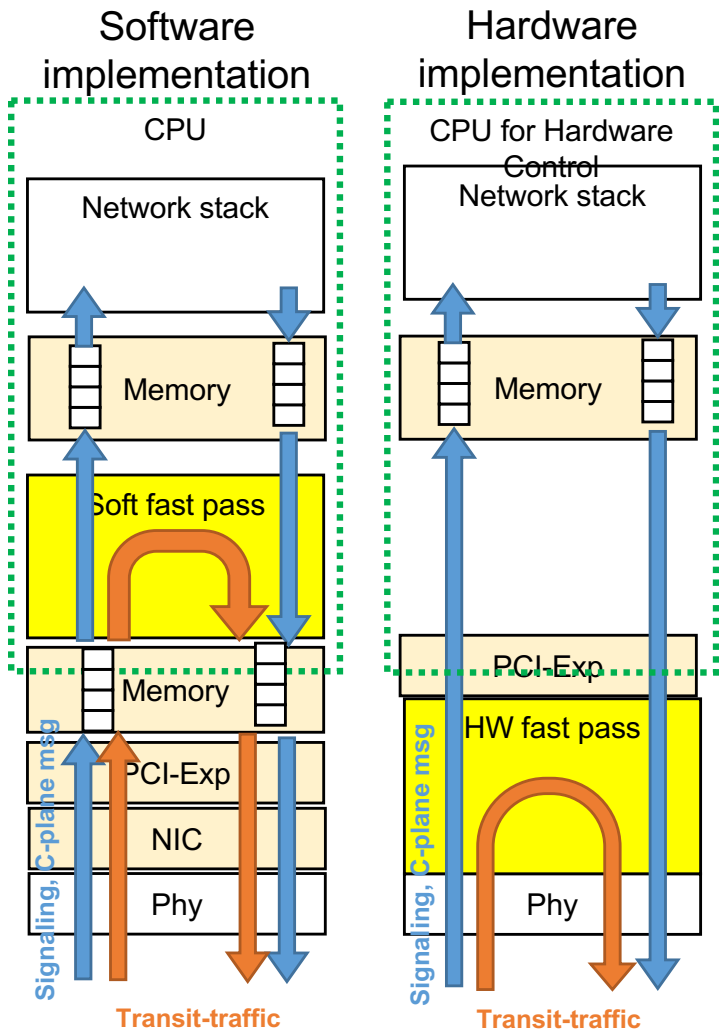
16 Gbps

800 Gbps

Signaling, C-plane msg

Transit-traffic

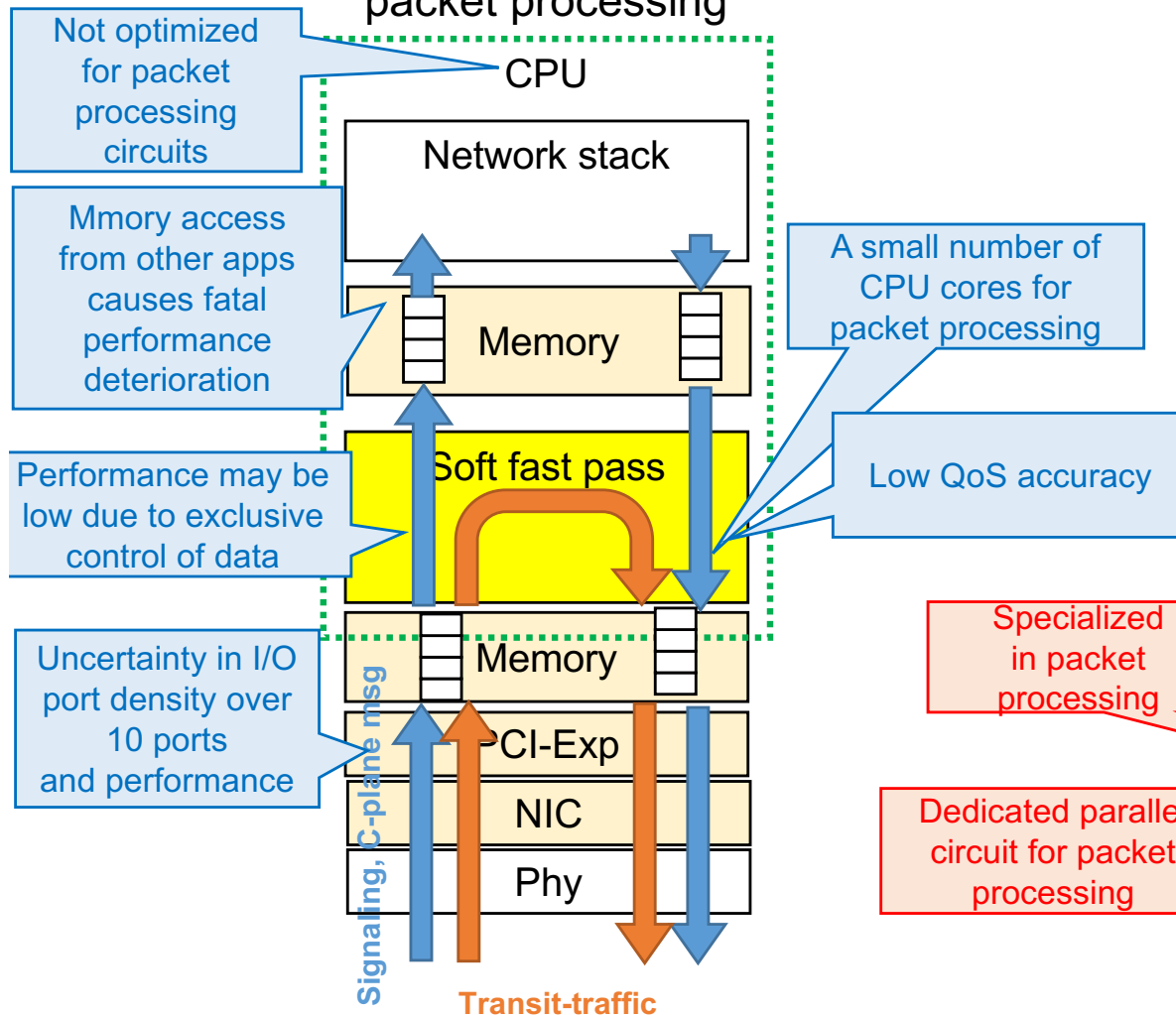
Specifications for each implementation



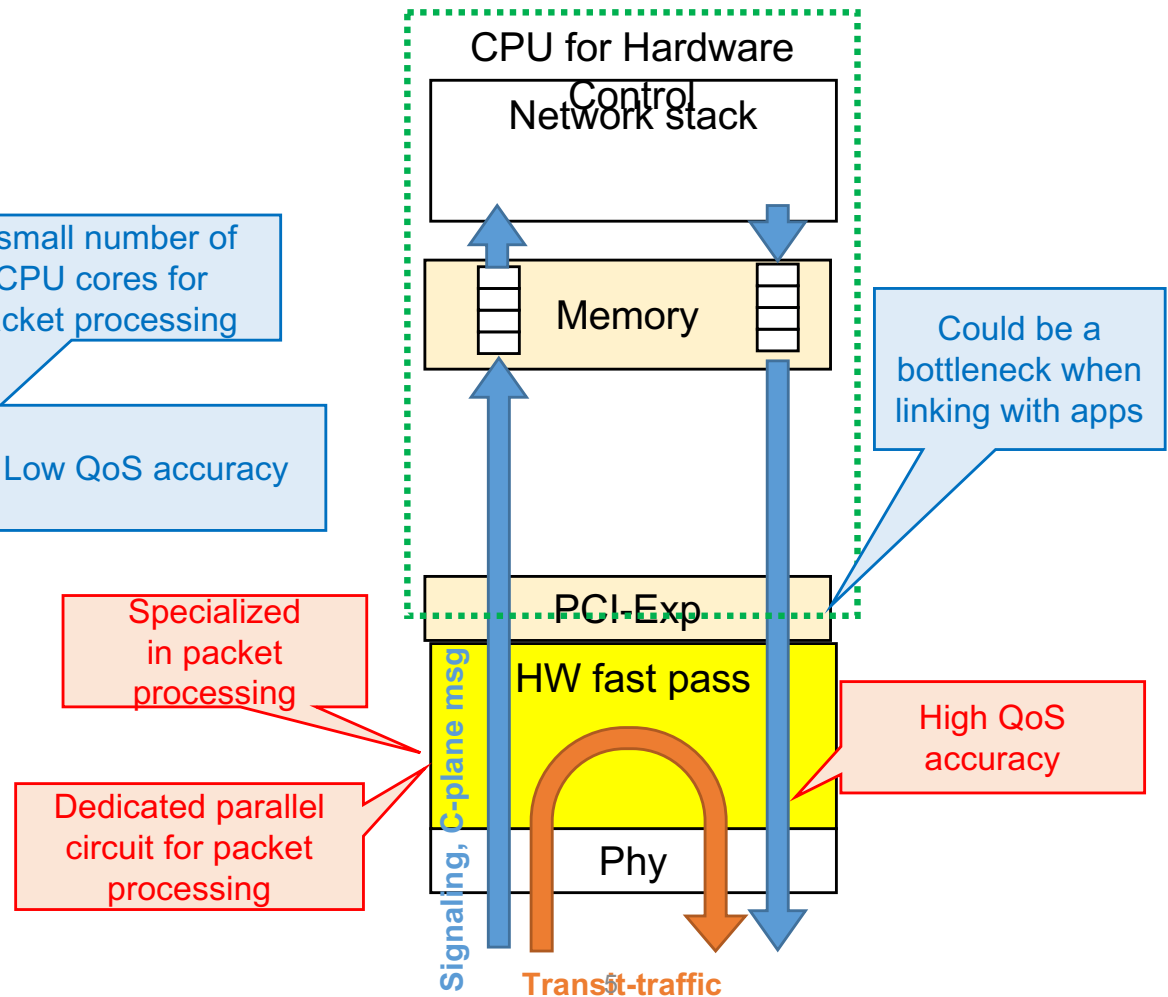
Type		Software implementation	Hardware implementation
C-plane	CPU	Latest Xeon class CPU can be used (TDP 150 W, 22 core)	Embedded low-power CPU (TDP 90 W, 8 core)
	Memory	16 GB or more	8-16 GB
	Storage	TB class also possible	100 GB class
Communication between C/D-planes		Inter-memory communication (400 Gbps class)	Via PCI-Exp
D-plane	Packet processing	Software processing via CPU	implemented by dedicated packet processing processor (NPU), FPGA, ASIC
	Throughput/chip	80 Gbps	800 Gbps/ASIC (BCM88670)
	Throughput/system	80 Gbps	3.2 Tbps/System (BCM88770)
	Latency	Tens of microseconds (ms)	Several microseconds (ms)
	IF speed	40Gbps	100Gbps
	Number of ports	10 ports/10GbE	100 ports/100GbE
	Phy	Via NIC/PCI-Exp	implemented by dedicated packet processing processor (NPU), FPGA, ASIC
	Power consumption	10–20 W/10GbE	Several watts/10GbE

Advantages and disadvantages from a performance point of view

Modern software implementation packet processing

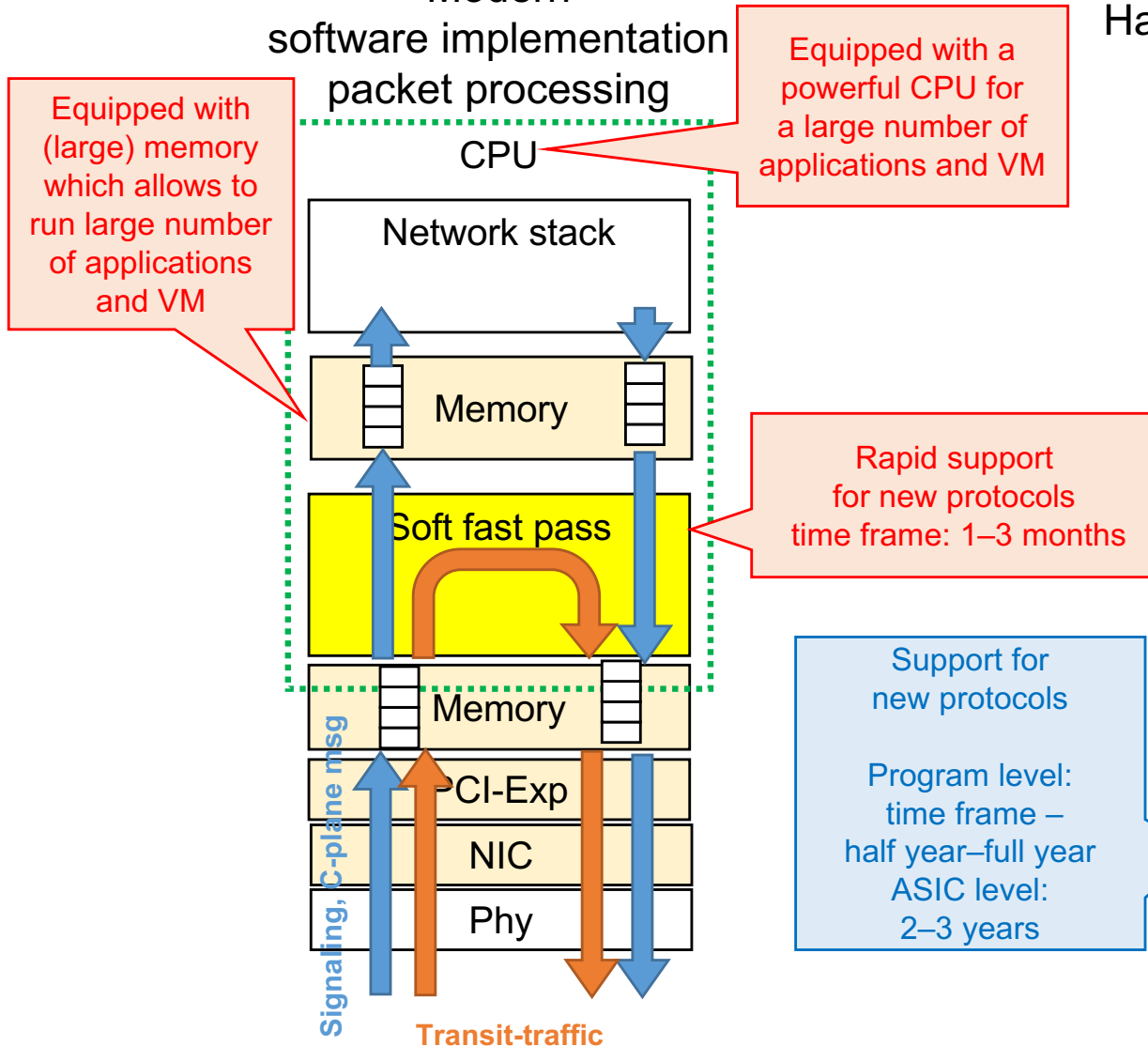


Hardware implementation packet processing

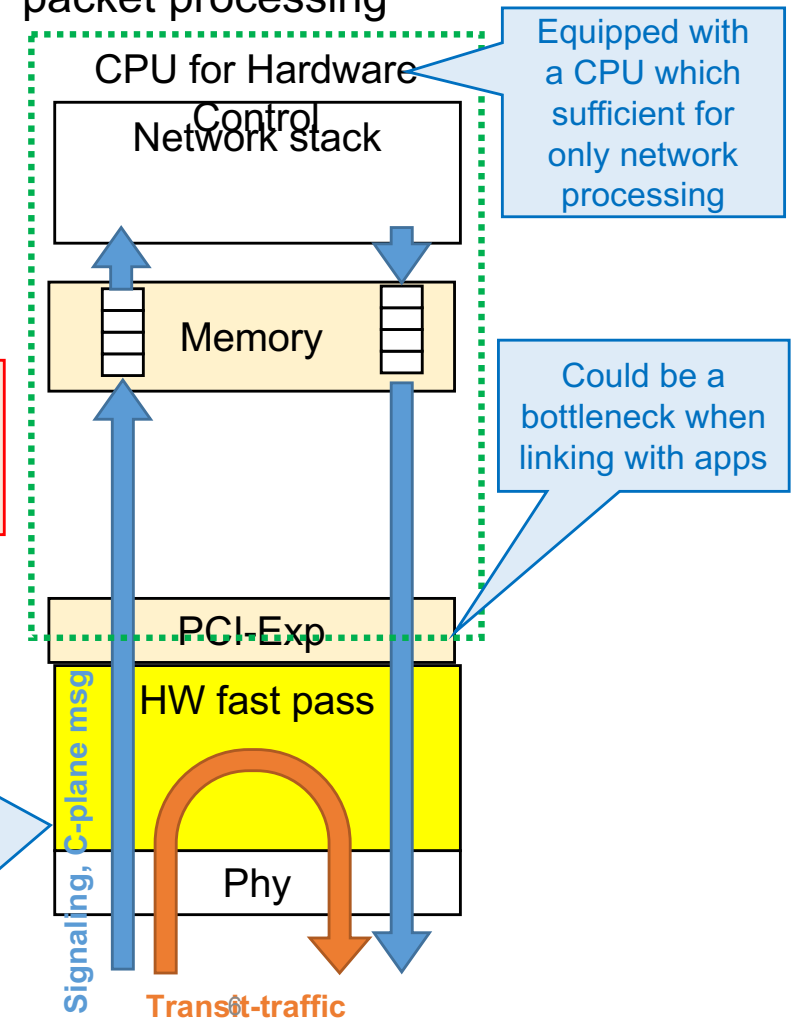


Advantages and disadvantages from an expandability point of view

Modern software implementation packet processing

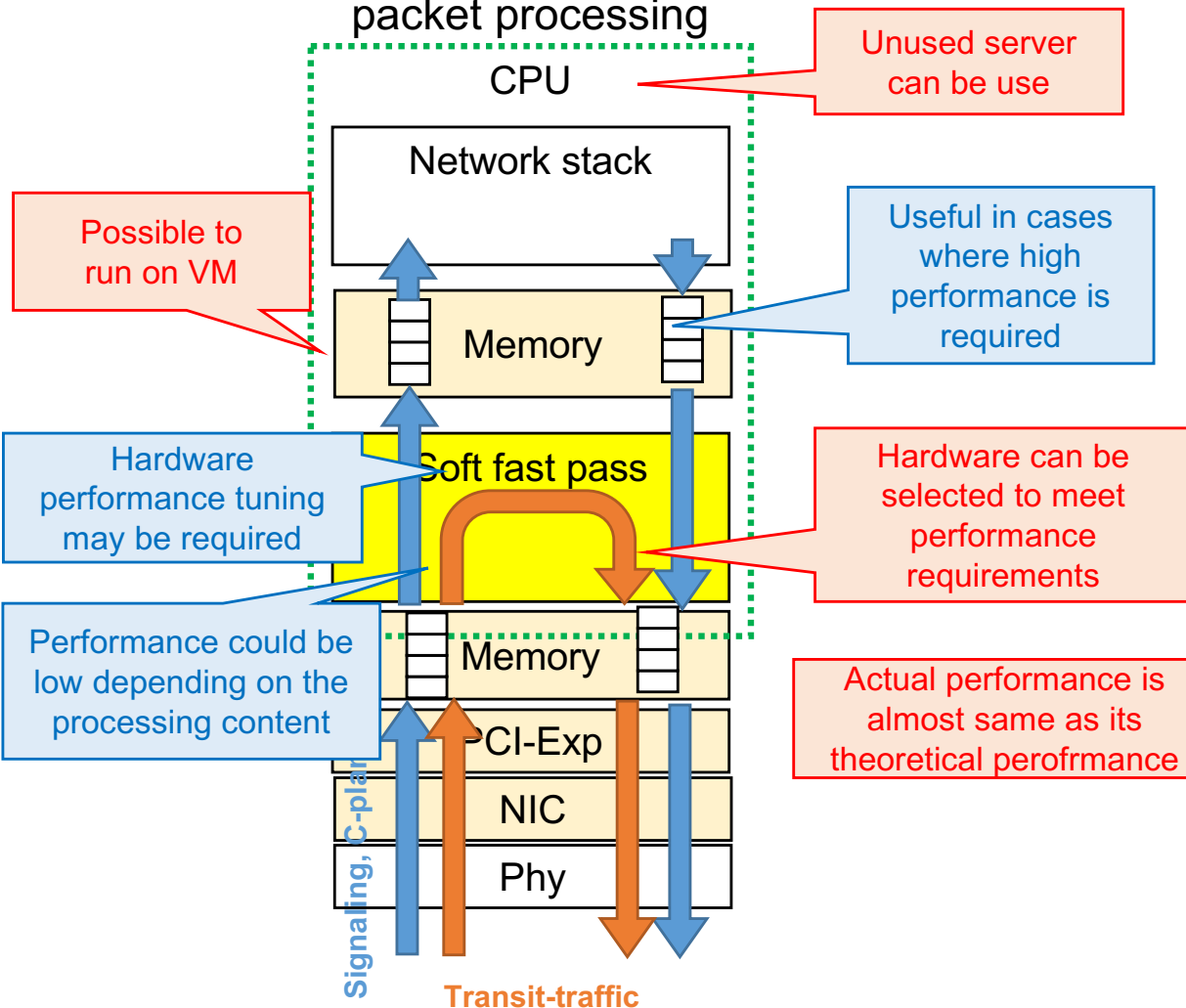


Hardware implementation packet processing

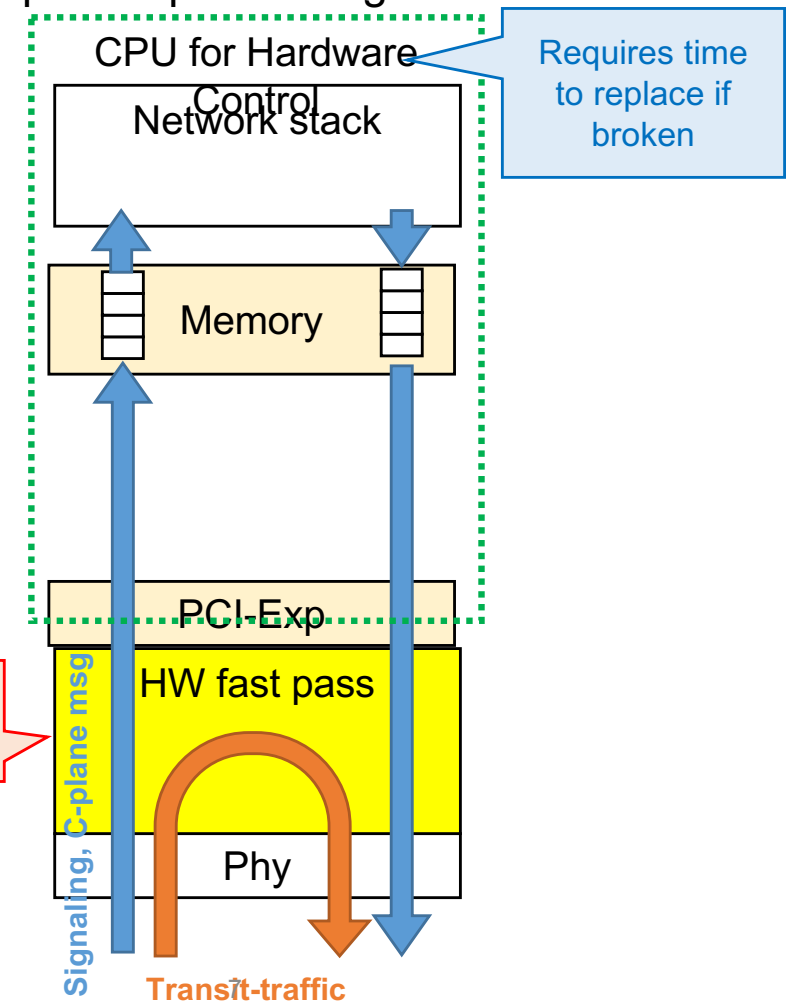


Advantages and disadvantages from an operational point of view

Modern software implementation packet processing



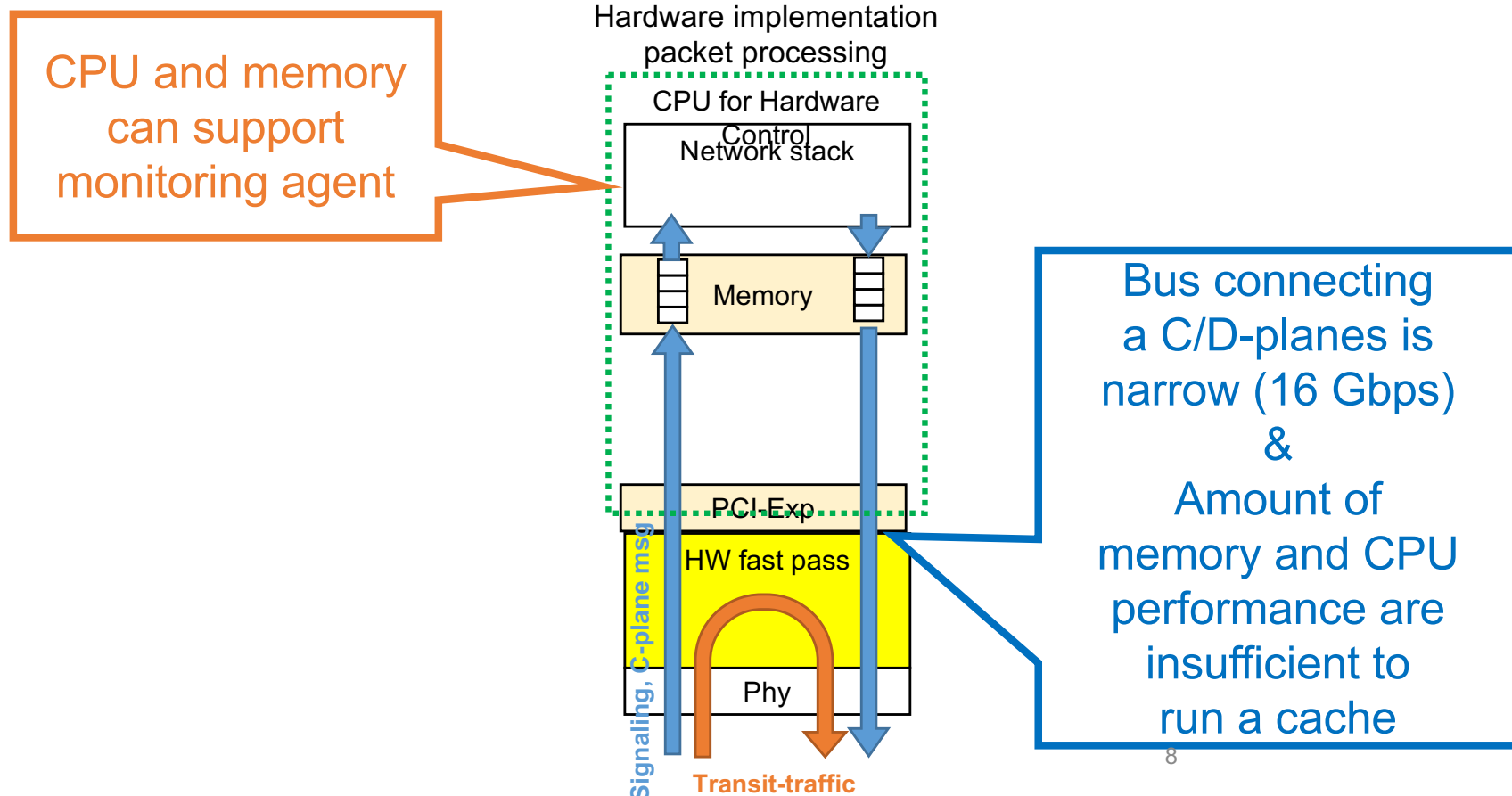
Hardware implementation packet processing



Back to original question #1

White-box switches (hardware implementation)

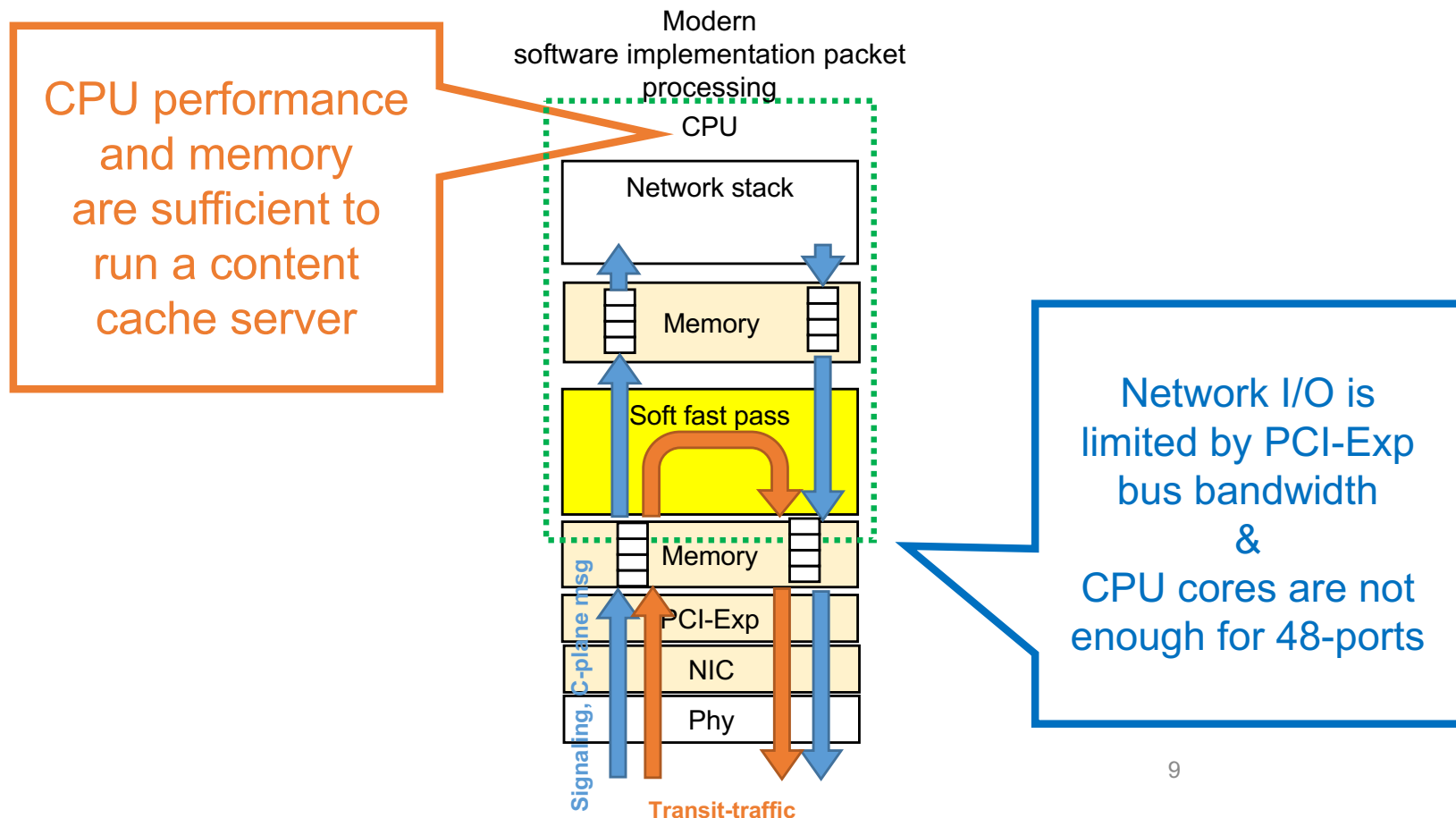
- Run a server/switch monitoring agent -> Yes
- Build a content cache server on Linux! -> No



Back to original question #2

Software router (software implementation)

- Run a content cache server together with the router -> Yes
- Run as a 48 ports ToR switch by plug in lots of NICs -> No



Summary

- Software implementation adaptive area
 - Adaptive area
 - Small to medium-sized edge routers
 - Gateways
 - Requirements:
 - Moderate performance (about 10 Gbps)
 - Number of ports: 6 ports
 - Number of required routes: 1 million or more
 - Advanced feature
- Hardware implementation adaptive areas
 - Adaptive area
 - ToR SW, aggregator SW
 - Core routers
 - Requirements:
 - Number of ports required
 - Tbps-class throughput
 - Low latency
 - Low power consumption