光トランシーバー制御信号解析のために
可視化ツールを作ってみたよ

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2022/1/28

● 名前

加藤利之(Toshiyuki Kato)

あだ名は「トッティ」、毎年箱根駅伝の観戦が楽しみ

● 職歴

国内半導体メーカーを経て、現在、株式会社マクニカで

光トランシーバーや光計測機器の技術サポートに従事

● 寄稿記事

月刊テレコミュニケーション「光トランシーバーと光伝送技術を徹底解剖」

https://businessnetwork.jp/Detail/tabid/65/artid/8667/Default.aspx

今回、お伝えしたいこと

- 3rd Party Opticsって、選択肢が多く、コストメリットもあります
- 導入時にトラブルが起きると、けっこう解決に時間がかかります
- そんなときに役に立つ時短ツールを紹介します

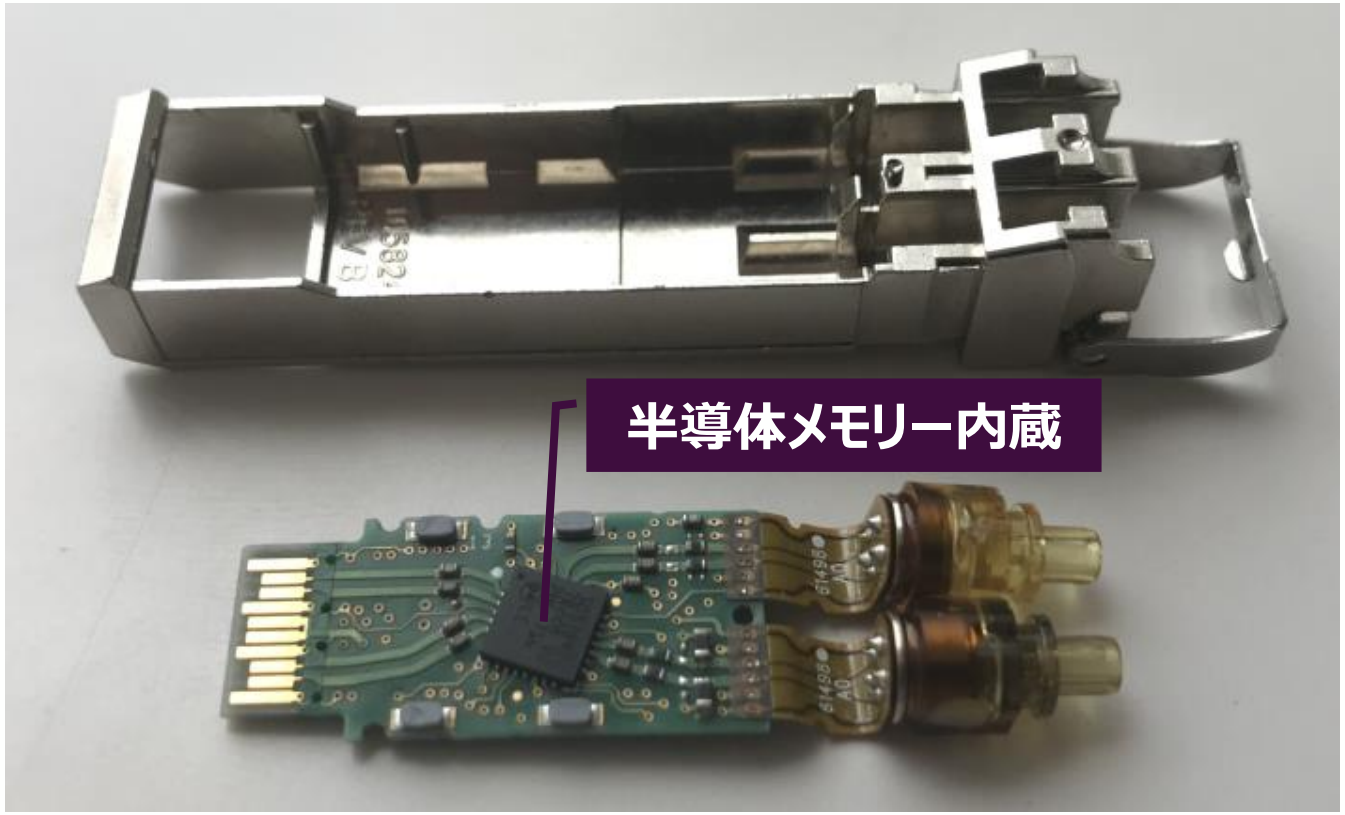
光トランシーバー制御信号解析

⇩

スイッチと光トランシーバーの会話を「のぞき見」して解析する

光トランシーバーには本人確認データが入っている

本人確認書類

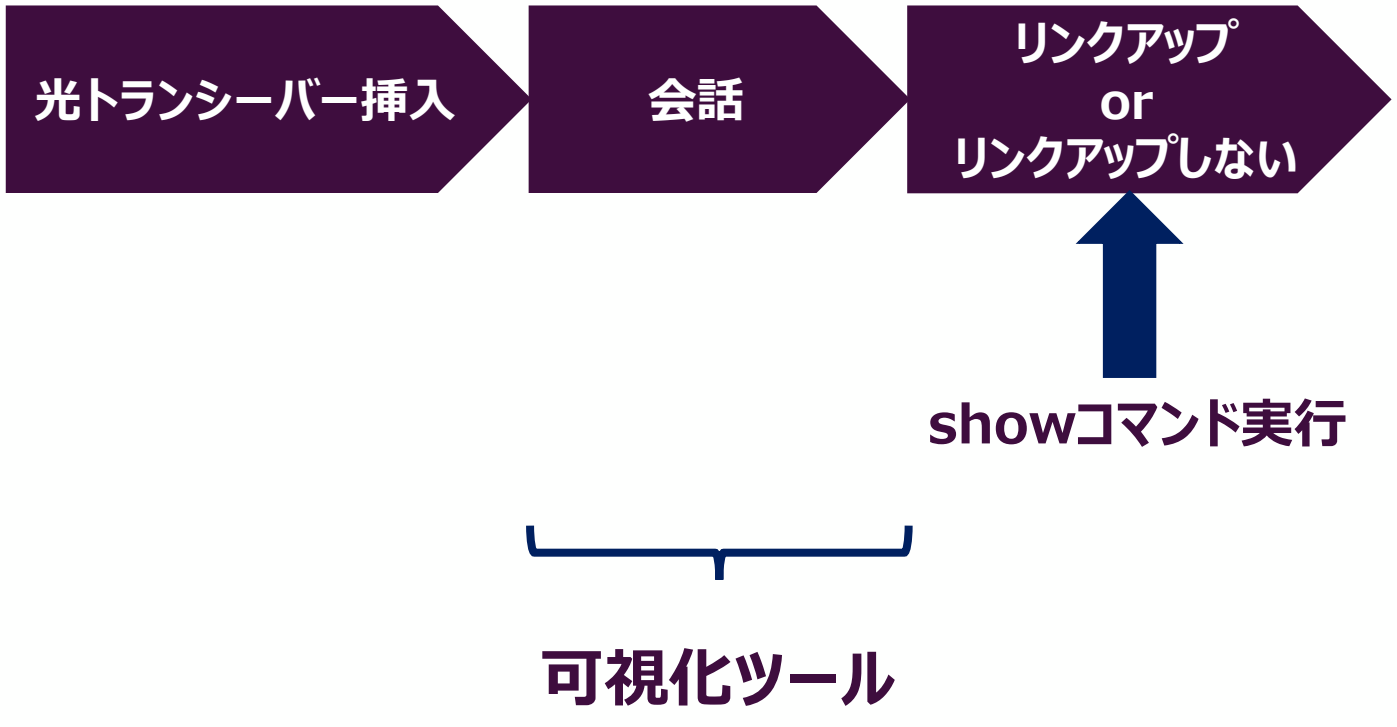


半導体メモリーに入っている情報

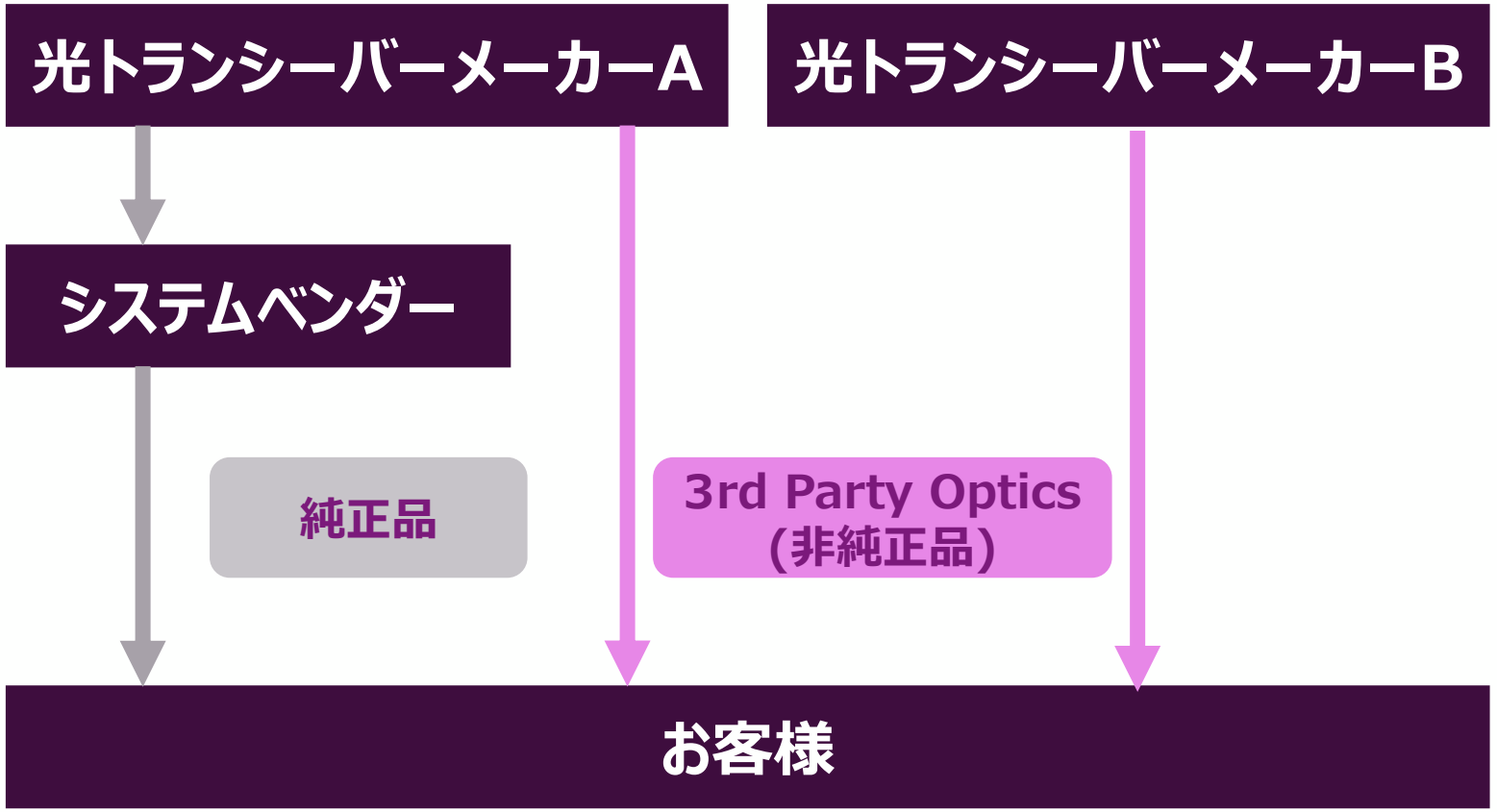
- ベンダー名
- 製品名
- シリアルナンバー
- 光トランシーバーモニター情報(光送信/受信パワーなど)

```
Ethtool Pluggables
------------------
        Identifier                                : 0x11 (QSFP28)
        Extended identifier                       : 0x8c
        Extended identifier description           : 2.5W max. Power consumption
        Extended identifier description           : CDR present in TX, CDR present in RX
        Extended identifier description           : High Power Class (> 3.5 W) not enabled
        Connector                                 : 0x0c (MPO Parallel Optic)
        Transceiver codes                         : 0x80 0x00 0x00 0x00 0x00 0x00 0x00 0x00
        Transceiver type                          : 100G Ethernet: 100G Base-SR4 or 25GBase-SR
        Encoding                                  : 0x07 ((256B/257B (transcoded FEC-enabled data))
        BR, Nominal                               : 25500Mbps
        Rate identifier                           : 0x00
        Length (SMF,km)                           : 0km
        Length (OM3 50um)                         : 70m
        Length (OM2 50um)                         : 0m
        Length (OM1 62.5um)                       : 0m
        Length (Copper or Active cable)           : 50m
        Transmitter technology                    : 0x00 (850 nm VCSEL)
        Laser wavelength                          : 850.000nm
        Laser wavelength tolerance                : 10.000nm
        Vendor name                               : xxxxxxxx
        Vendor OUI                                : 00:90:65
        Vendor PN                                 : xxxxxxxx
        Vendor rev                                : xxxxxxxx
        Vendor SN                                 : xxxxxxxx
        Revision Compliance                       : Unallocated
        Module temperature                        : 27.61 degrees C / 81.69 degrees F
        Module voltage                            : 3.2553 V
        Alarm/warning flags implemented           : Yes
        Laser tx bias current (Channel 1)         : 8.480 mA
        Laser tx bias current (Channel 2)         : 8.418 mA
        Laser tx bias current (Channel 3)         : 8.480 mA
        Laser tx bias current (Channel 4)         : 8.480 mA
        Transmit avg optical power (Channel 1)    : 1.0805 mW / 0.34 dBm
        Transmit avg optical power (Channel 2)    : 1.0601 mW / 0.25 dBm
        Transmit avg optical power (Channel 3)    : 1.0456 mW / 0.19 dBm
        Transmit avg optical power (Channel 4)    : 1.0718 mW / 0.30 dBm
        Rcvr signal avg optical power(Channel 1)  : 0.9798 mW / -0.09 dBm
        Rcvr signal avg optical power(Channel 2)  : 1.0156 mW / 0.07 dBm
        Rcvr signal avg optical power(Channel 3)  : 0.6623 mW / -1.79 dBm
        Rcvr signal avg optical power(Channel 4)  : 0.9690 mW / -0.14 dBm
```

スイッチのShowコマンド(例)

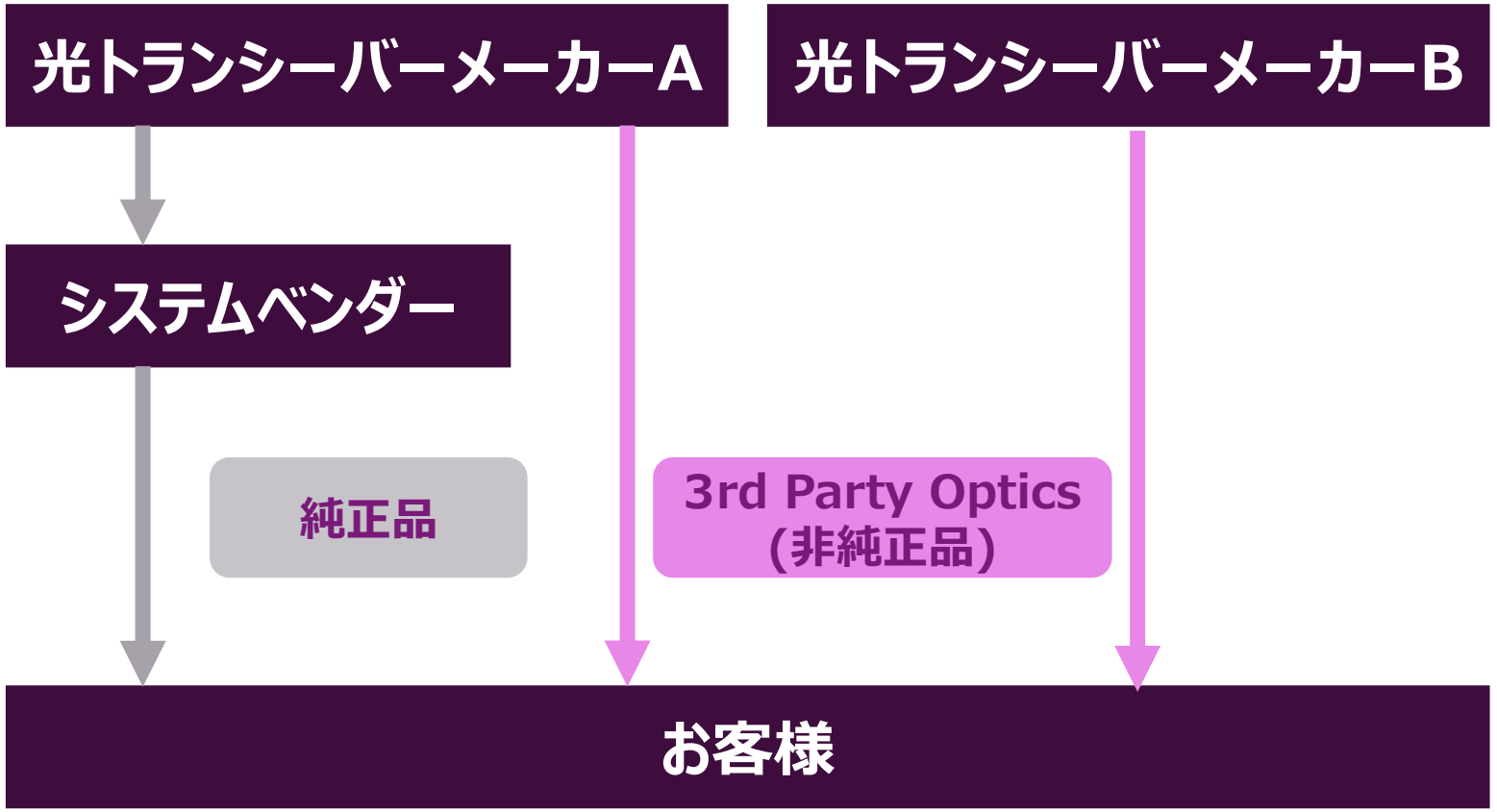


3rd Party Optics導入のメリットと課題



・安価で豊富なラインアップから選択できる
・「機器としての管理」から「消耗品としての取り扱い」にできる

3rd Party Optics導入のメリットと課題



・システムベンダーからのサポートに頼らない運用が必要

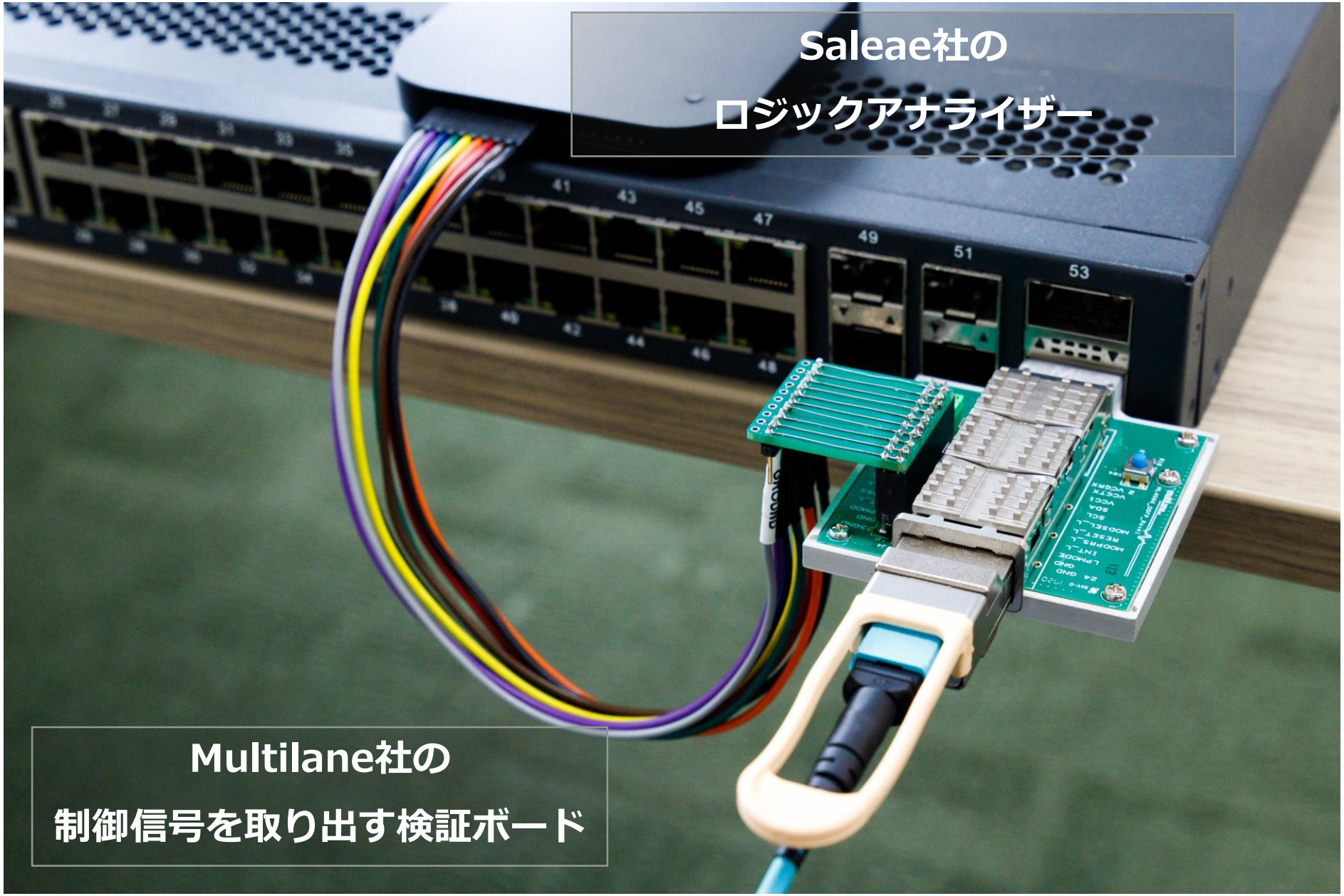
3rd Party Optics導入時によくあるリンクアップしない事例

ハード要因

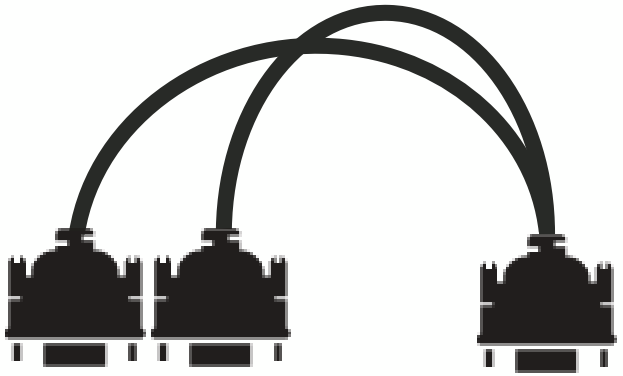
- 光コネクターの端面汚れ
- 初期故障(レーザー、電子部品等)　・・・ごく稀です

ソフト要因

- 光トランシーバーの設定(Configuration)まちがい

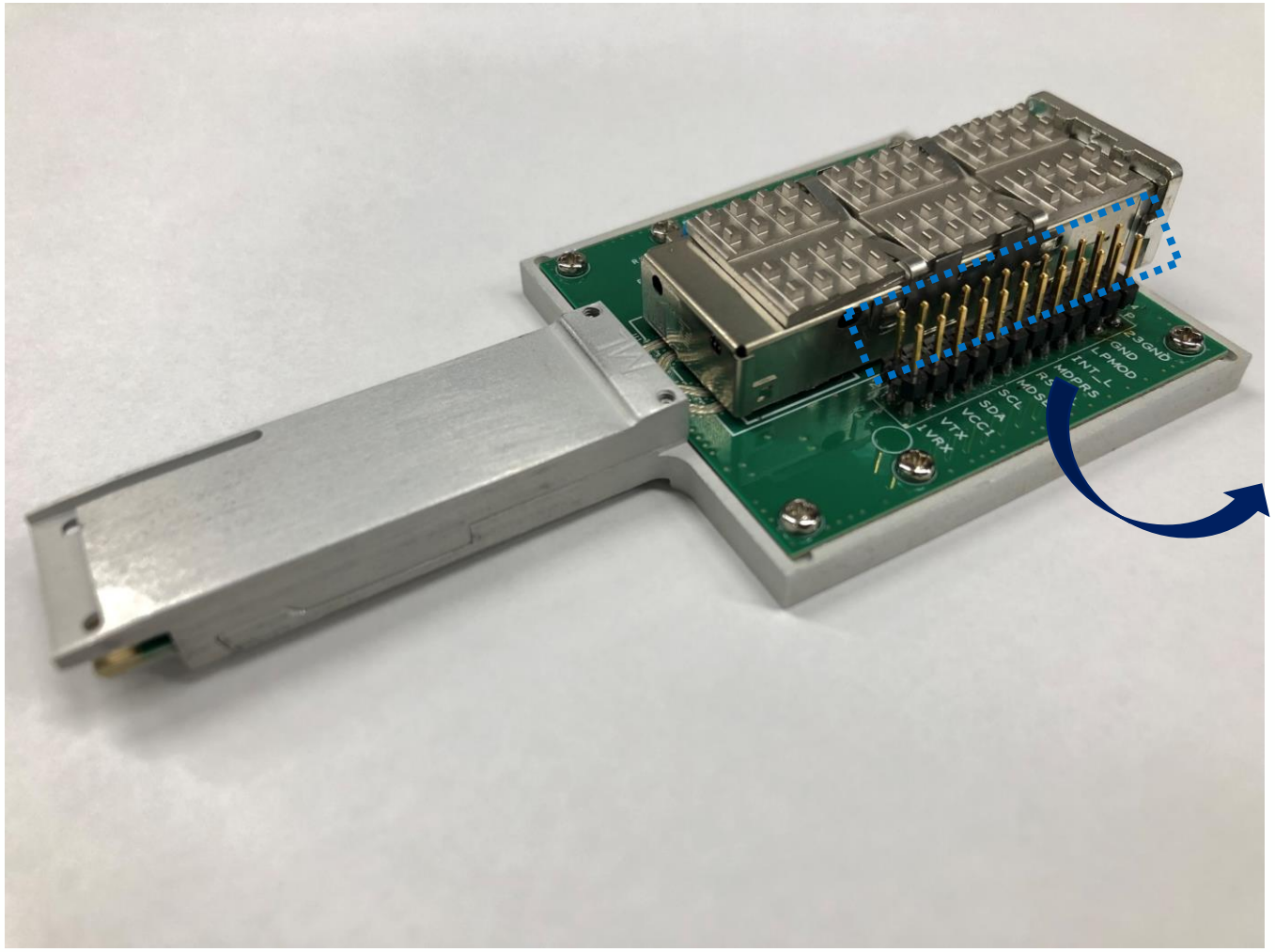


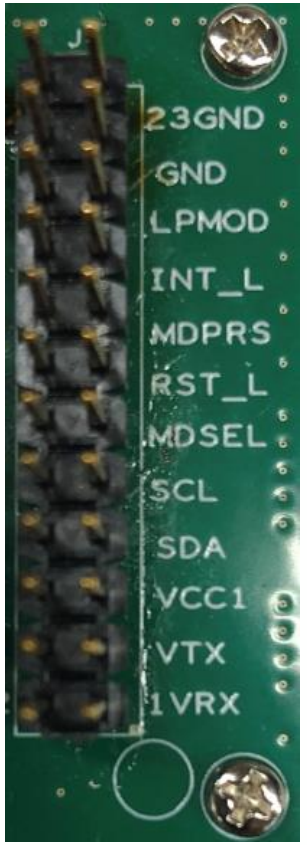
光トランシーバー



2出力　　1入力

VGAケーブル



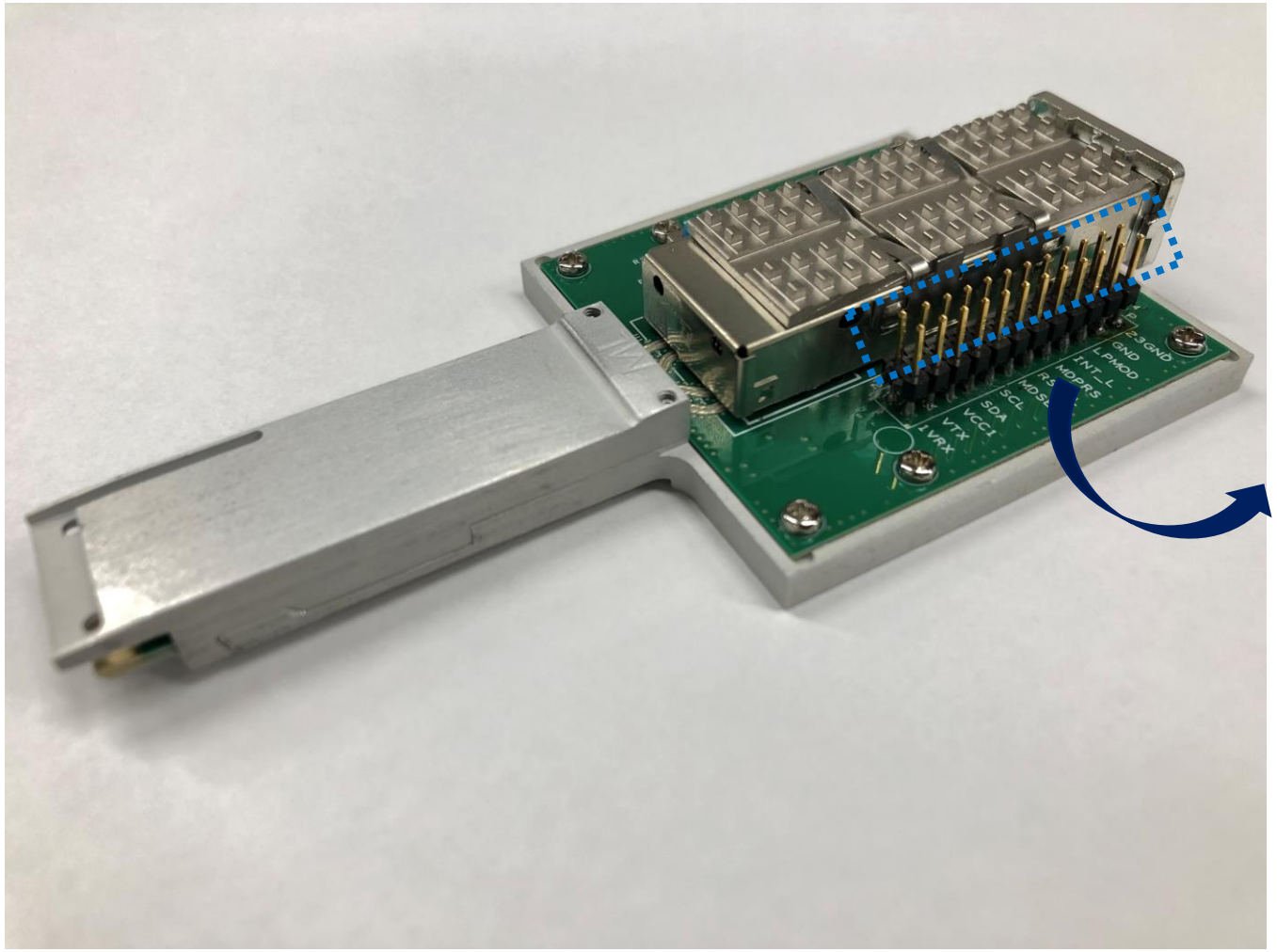


ネットワーク機器

制御信号

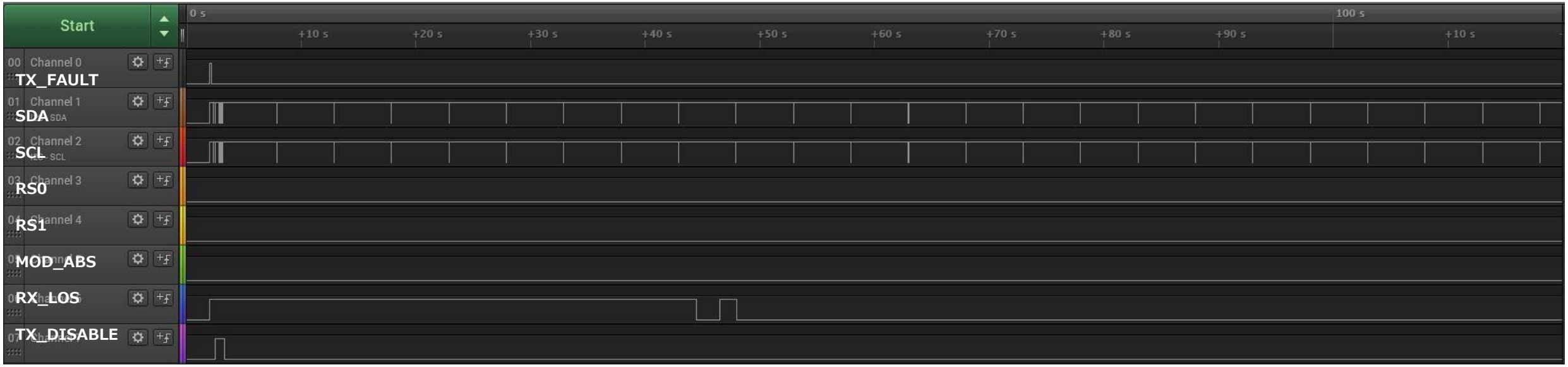
GND	Ground
LPMOD	Low Power Mode
INT_L	Interrupt
MDPRS	Module Present
RST_L	Module Reset
MDSEL	Module Select
SCL	I2C(Clock)
SDA	I2C(Data)
VCC	Power Supply

光トランシーバー



ネットワーク機器

Low or High ?



時間

リンクアップしない

ネットワーク機器の制御信号取得

ログ出力(ロジアナ)

Write/Read　レジスター調査

SFF規格書で該当レジスター確認

Write/Read内容把握

```
NAME: "HundredGigE0/0/1/0", DESCR: "QSFP28 100G SR4 Pluggable Optics Module"

RP/0/RP0/CPU0:xxxxxx#show interfaces hundredGigE 0/0/1/0
HundredGigE0/0/1/0 is down, line protocol is down

State:
   Administrative state: enabled
   Operational state: Down (Reason: Link loss or low light, no loopback)
   LED state: Yellow On

Phy:
   Media type: fiber over 4 lane optics (short reach)
   Optics:
      Vendor: xxxxxxx
      Part number: xxxxxxxx
      Serial number: xxxxxxx
      Wavelength: 850 nm
   Digital Optical Monitoring:
      Transceiver Temp: 31.183 C
      Transceiver Voltage: 3.271 V

Wavelength    Tx Power        Rx Power      Laser Bias
      Lane  (nm)    (dBm)    (mW)    (dBm)    (mW)     (mA)
      --    -----   ------   ------   ------   ------   ------
      0     n/a     0.1    1.0158     0.1    1.0219     8.370
      1     n/a     0.3    1.0780    -0.4    0.9108     8.370
      2     n/a     0.2    1.0551    -0.3    0.9389     8.432
      3     n/a     0.3    1.0629    -0.5    0.8927     8.432

Alarms:
      Current:
         No alarms
```

リンクアップしない

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ネットワーク機器の制御信号取得

↓

ログ出力(ロジアナ)

↓

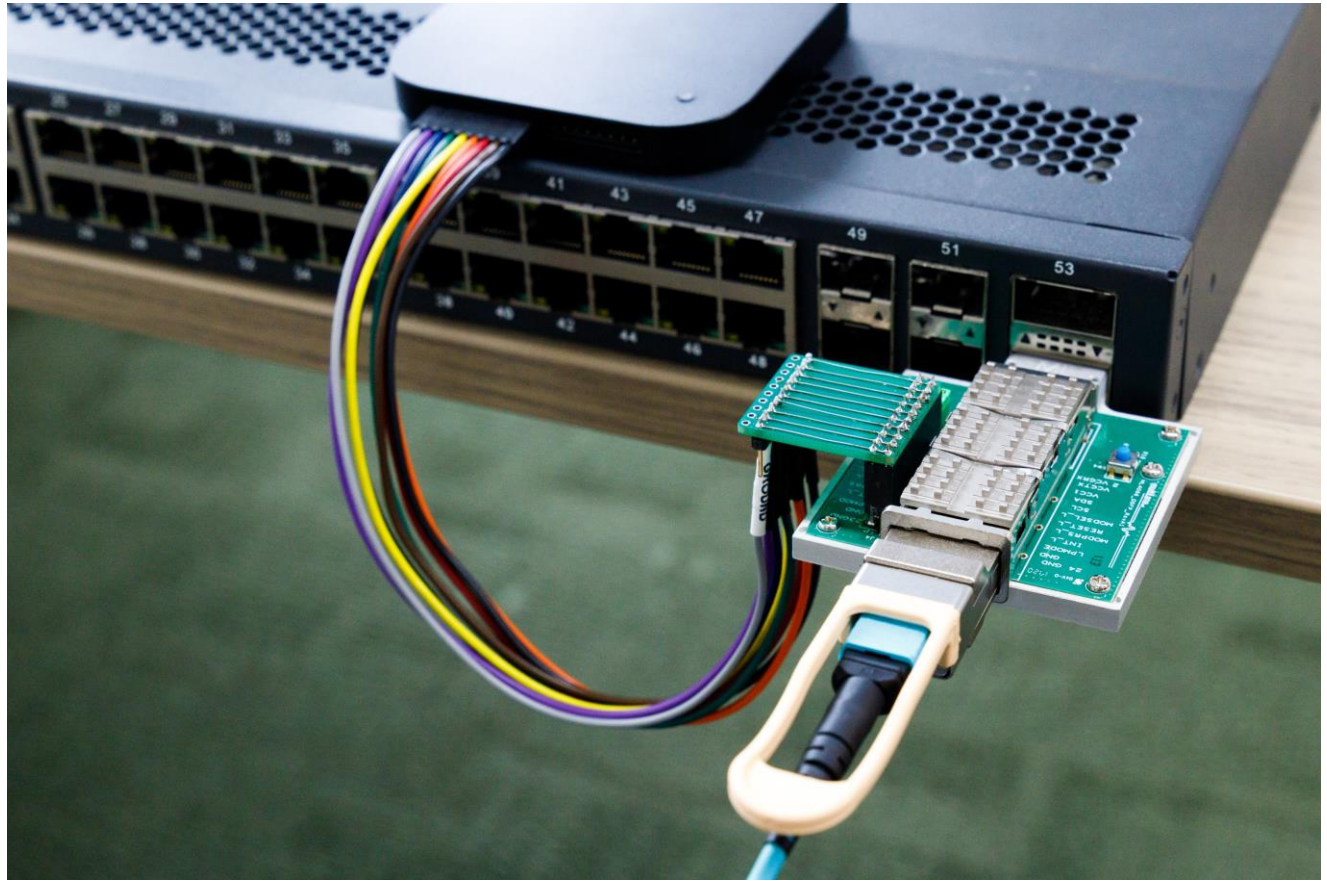
Write/Read　レジスター調査

↓

SFF規格書で該当レジスター確認

↓

Write/Read内容把握



リンクアップしない

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ネットワーク機器の制御信号取得

↓

ログ出力(ロジアナ)

↓

Write/Read　レジスター調査

↓

SFF規格書で該当レジスター確認

↓

Write/Read内容把握

リンクアップしない

↓

ネットワーク機器の制御信号取得

↓

ログ出力(ロジアナ)

↓

Write/Read　レジスター調査

↓

SFF規格書で該当レジスター確認

↓

Write/Read内容把握

```
831 Setup Read to ['163' (0xA3)] + ACK
832 '8' (0x08) + NAK
833 Setup Write to ['226' (0xE2)] + ACK
834 '6' (0x06) + ACK
835 Setup Write to ['162' (0xA2)] + ACK
836 v (0x76) + ACK
837 Setup Read to ['163' (0xA3)] + ACK
838 '11' (0x0B) + NAK
839 Setup Write to ['226' (0xE2)] + ACK
840 '6' (0x06) + ACK
841 Setup Write to ['162' (0xA2)] + ACK
842 n (0x6E) + ACK
843 Setup Read to ['163' (0xA3)] + ACK
844 '8' (0x08) + NAK
845 Setup Write to ['226' (0xE2)] + ACK
846 '6' (0x06) + ACK
847 Setup Write to ['162' (0xA2)] + ACK
848 v (0x76) + ACK
849 Setup Read to ['163' (0xA3)] + ACK
850 '11' (0x0B) + NAK
851 Setup Write to ['226' (0xE2)] + ACK
852 '6' (0x06) + ACK
853 Setup Write to ['162' (0xA2)] + ACK
854 n (0x6E) + ACK
855 Setup Read to ['163' (0xA3)] + ACK
856 '8' (0x08) + NAK
```

ネットワーク機器からの
I2C制御信号を抽出
かなりの量・・・

リンクアップしない

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ネットワーク機器の制御信号取得

↓

ログ出力(ロジアナ)

↓

Write/Read　レジスター調査

↓

SFF規格書で該当レジスター確認

↓

Write/Read内容把握

・
・
・
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・
・

Byte 238
0x00
Byte 239
0x00

・
・
・
・
・

Writeコマンド発見！

リンクアップしない

↓

ネットワーク機器の制御信号取得

↓

ログ出力(ロジアナ)

↓

Write/Read　レジスター調査

↓

SFF規格書で該当レジスター確認

↓

Write/Read内容把握

SFF-8636

6.6.3 Optional Channel Controls (Page 03h, Bytes 230-241)

Upper Memory Page Control Bits are used to define the optional channel controls.

Table 6-29 Optional Channel Controls (Page 03h Bytes 230-241)

Byte	Bit	Name	Description	PC	AC	AO	SM
230	7	Host-Side FEC enable	Enables host-side FEC termination on the Tx electrical inputs and host-side FEC generation on the Rx electrical outputs. 0b = disable, 1b = enable. Default = 0.	-	O	O	O
	6	Media-Side FEC enable	Enables media-side FEC generation on the Tx outputs and media-side FEC termination on the Rx inputs. 0b = enable, 1b = disable. Default = 0.	-	O	O	O
	5-0	Reserved		-	-	-	-
231	7-4	Reserved		-	-	-	-
	3	Tx4 Force Squelch	Software squelch of transmitter output, per media lane. Note that the transmitter output may be disabled, which overrides the behaviors of this control 0b = No impact on Tx behavior 1b = Tx output squelched See Page 03h Byte 227 bit 3 for implementation indicator.	-	O	O	O
	2	Tx3 Force Squelch		-	O	O	O
	1	Tx2 Force Squelch		-	O	O	O
	0	Tx1 Force Squelch		-	O	O	O
232	All	Reserved		-	-	-	-
233	7-4	Reserved		-	-	-	-
	3	Tx1AEFreeze	Controls to freeze Tx input adaptive equalizers. 1 to freeze, else 0. See page 00h byte 193 bit 4 for support indicator.	O	O	O	O
	2	Tx2AEFreeze		O	O	O	O
	1	Tx3AEFreeze		O	O	O	O
	0	Tx4AEFreeze		O	O	O	O
234	7-4	Tx1 input equalizer control	Tx input equalizer controls (see Page	O	O	O	O
237	7-4	Rx3 output emphasis control		O	O	O	O
	3-0	Rx4 output emphasis control		O	O	O	O
238	7-4	Rx1 output amplitude control	Controls for Rx output differential amplitude. (See Table 6-30)	O	O	O	O
	3-0	Rx2 output amplitude control		O	O	O	O
239	7-4	Rx3 output amplitude control		O	O	O	O
	3-0	Rx4 output amplitude control		O	O	O	O
240	7	Rx4 SQ Disable	Controls to disable squelch of Rx outputs. 1 = Disabled, 0 = Enabled Default = 0.	O	O	O	O
	6	Rx3 SQ Disable		O	O	O	O
	5	Rx2 SQ Disable		O	O	O	O
	4	Rx1 SQ Disable		O	O	O	O
	3	Tx4 SQ Disable	Controls to disable squelch of Tx outputs. 1 = Disabled, 0 = Enabled Default = 0.	O	O	O	O
	2	Tx3 SQ Disable		O	O	O	O
	1	Tx2 SQ Disable		O	O	O	O
	0	Tx1 SQ Disable		O	O	O	O
241	7	Rx4 Output Disable	Controls to disable Rx outputs. 1 = Disabled, 0 = Enabled Default = 0.	O	O	O	O
	6	Rx3 Output Disable		O	O	O	O
	5	Rx2 Output Disable		O	O	O	O
	4	Rx1 Output Disable		O	O	O	O
	3	Tx4 adaptive equalization control	Controls for Tx input adaptive equalizers. 1b=Enable (default) 0b=Disable (use manual EQ) See 00h 193 bit 3 for implementation indicator.	-	O	O	O
	2	Tx3 adaptive equalization control		-	O	O	O
	1	Tx2 adaptive equalization control		-	O	O	O
	0	Tx1 adaptive equalization control		-	O	O	O

引用元 https://members.snia.org/document/dl/26418

リンクアップしない

↓

ネットワーク機器の制御信号取得

↓

ログ出力(ロジアナ)

↓

Write/Read　レジスター調査

↓

SFF規格書で該当レジスター確認

↓

Write/Read内容把握

Default設定(赤枠)

Table 6-30 Output Differential Amplitude Control (Page 03h Bytes 238-239)

Value	Receiver Output Amplitude No Output Equalization	
	Nominal	Units
1xxxb	Reserved	
0111b		
0110b		
0101b		
0100b		
0011b	600-1200	mV (p-p)
0010b	400-800	
0001b	300-600	
0000b	100-400	

引用元 https://members.snia.org/document/dl/26418

リンクアップしない

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ネットワーク機器の制御信号取得

↓

ログ出力(ロジアナ)

↓

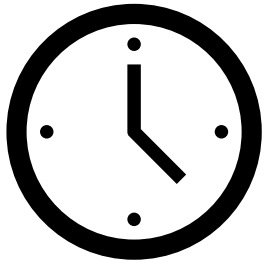
Write/Read　レジスター調査

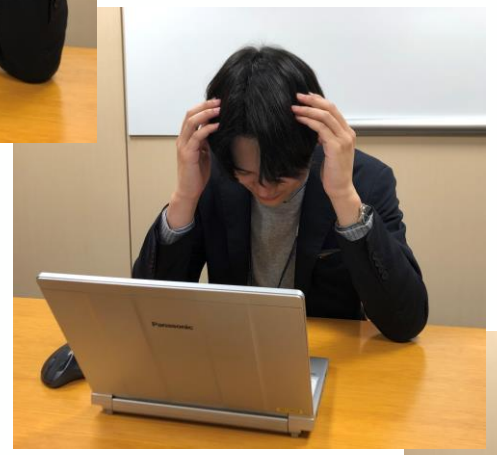
↓

SFF規格書で該当レジスター確認

↓

Write/Read内容把握





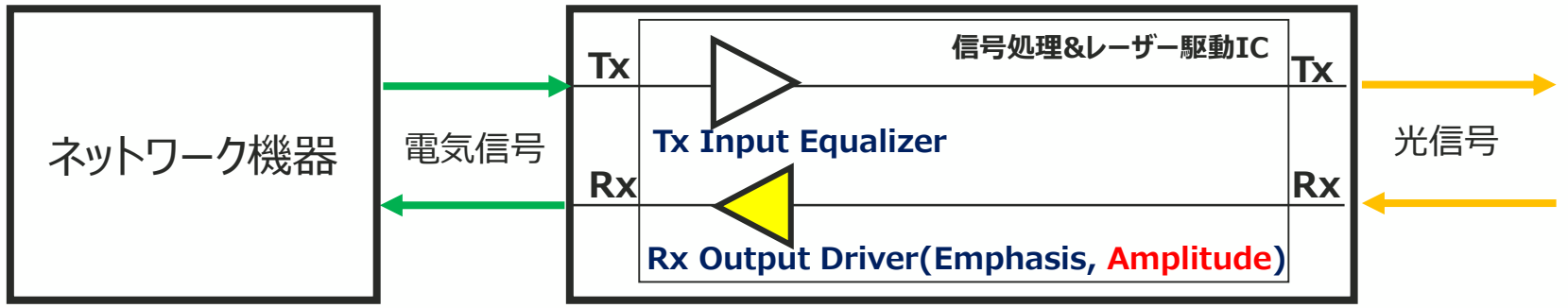

I2C Analyzer for JANOG49
ファイル
ホーム
共有
表示
PC › デスクトップ › I2C Analyzer for JANOG49
名前
更新日時
種類
サイズ
img
2022/01/12 14:20
ファイル フォルダー
js
2022/01/11 13:33
ファイル フォルダー
2022/01/11 13:30
JPG ファイル
5 KB
index.html
2022/01/12 14:21
Chrome HTML Do...
4 KB
Index.html ダブルクリック

Relative time [ms]	Command	Address dec	Data hex	Page number	Meaning	Details
0	Write/Address	0		0		
0.225	Read	0	0x11		Vendor Specific	*Description of Module, with memory map type if not unique [0x11] QSFP28 or later with SFF-8636 management interface. (SFF-8665 et al.) 0x11 may prevent the use of new 25G-class modules on old hosts. Not recommended for new designs
0.471	Write/Address	1		0		
0.696	Read	1	0x07	0	Vendor Specific	*Revision Compliance, Memory Map Version [0x07] SFF-8636 Rev 2.5, 2.6 and 2.7
0.941	Write/Address	2		0		
1.166	Read	2	0x00	0	Vendor Specific	Bit 7-4 = [0000] Reserved. Module State Code – reserved for microQSFP MSA. Bit 3 = [0] Reserved. *Flat_mem, Upper memory flat or paged. See Page 00h, Byte 195 for additional advertising. Bit 2 = [0] Paging (at least upper page 03h implemented) *IntL, Digital state of the IntL Interrupt output pin. Default = 1. Bit 1 = [0] IntL asserted. *Data_Not_Ready, Indicates free-side does not yet have valid monitor data. The bit remains high until valid data can be read at which time the bit goes low. Bit 0 = [0] Valid data is ready.
1.412	Write/Address	3		0		
						*Latched LOS indicator

Relative time [ms]	Command	Address dec	Data hex	Page number	Meaning	Details
4,645.112	Write/Data	245	0x00	3	Channel Monitor Masks	Bit 6 = [0] M-Tx3 Bias Low Alarm Bit 5 = [0] M-Tx3 Bias High Warning Bit 4 = [0] M-Tx3 Bias Low Warning Bit 3 = [0] M-Tx4 Bias High Alarm [0] M-Tx4 Bias Low Alarm [0] M-Tx4 Bias High Warning Bit 0 = [0] M-Tx4 Bias Low Warning
5,147.637	Write/Data	234	0x00	3	Optional Channel Controls	*Tx1 input equalizer control, Tx input equalizer controls (see Page 03h Byte 224 and Table 6-31) Bit 7-4 = [0000] 0 dB (No EQ) *Tx2 input equalizer control, Tx input equalizer controls (see Page 03h Byte 224 and Table 6-31) Bit 3-0 = [0000] 0 dB (No EQ)
5,197.988	Write/Data	235	0x00	3	Optional Channel Controls	*Tx3 input equalizer control, Tx input equalizer controls (see Page 03h Byte 224 and Table 6-31) Bit 7-4 = [0000] 0 dB (No EQ) *Tx4 input equalizer control, Tx input equalizer controls (see Page 03h Byte 224 and Table 6-31) Bit 3-0 = [0000] 0 dB (No EQ)
5,248.339	Write/Data	236	0x00	3	Optional Channel Controls	*Rx1 output emphasis control, Rx output emphasis controls (see Page 03h Byte 224 and Table 6-32) Bit 7-4 = [0000] 0 dB (No Emphasis) *Rx2 output emphasis control, Rx output emphasis controls (see Page 03h Byte 224 and Table 6-32) Bit 3-0 = [0000] 0 dB (No Emphasis)
5,298.69	Write/Data	237	0x00	3	Optional Channel Controls	*Rx3 output emphasis control, Rx output emphasis controls (see Page 03h Byte 224 and Table 6-32) Bit 7-4 = [0000] 0 dB (No Emphasis) *Rx4 output emphasis control, Rx output emphasis controls (see Page 03h Byte 224 and Table 6-32) Bit 3-0 = [0000] 0 dB (No Emphasis)
5,349.042	Write/Data	238	0x22	3	Optional Channel Controls	*Rx1 output amplitude control, Controls for Rx output differential amplitude. (See Table 6-30) Bit 7-4 = [0010] 400-800 mV(p-p) *Rx2 output amplitude control, Controls for Rx output differential amplitude. (See Table 6-30) Bit 3-0 = [0010] 400-800 mV(p-p)
5,399.393	Write/Data	239	0x22	3	Optional Channel Controls	*Rx3 output amplitude control, Controls for Rx output differential amplitude. (See Table 6-30) Bit 7-4 = [0010] 400-800 mV(p-p) *Rx4 output amplitude control, Controls for Rx output differential amplitude. (See Table 6-30) Bit 3-0 = [0010] 400-800 mV(p-p)
5,500.096	Write/Data	86	0x00	0	Vendor Specific	Bit 7-4 = [0000] Reserved *Read/Write bit for software disable of Tx For the case of an electrical/optical transceiver, writing [1] disables the laser of the channel Bit 3 = [0] Tx4 Disable (0:Enable/1:Disable) Bit 2 = [0] Tx3 Disable (0:Enable/1:Disable)

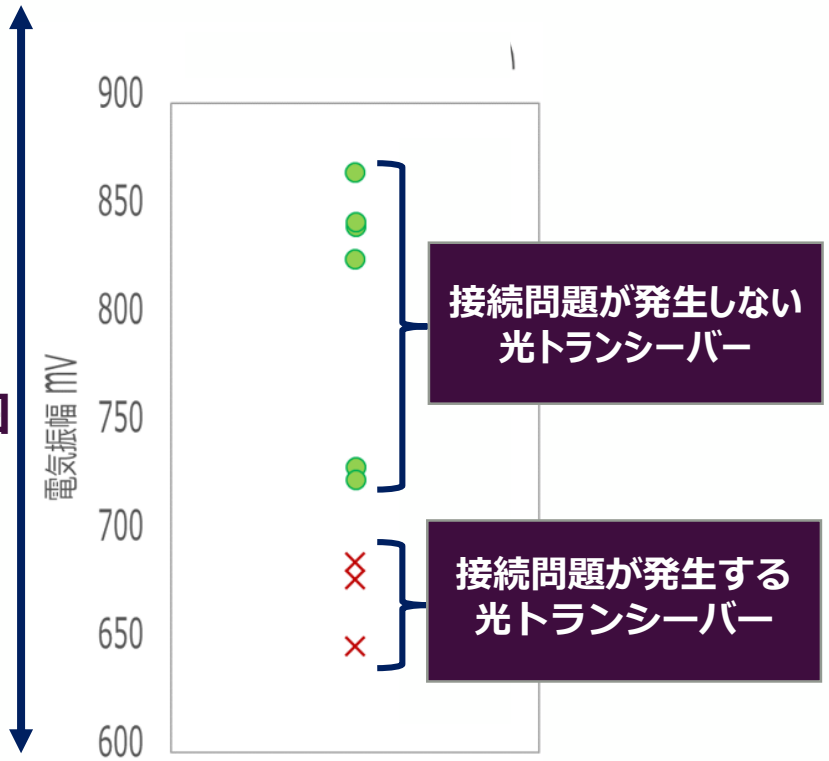
Tx Equalizerゼロ設定

ネットワーク装置に渡す電気信号の振幅を最大に設定していたケース

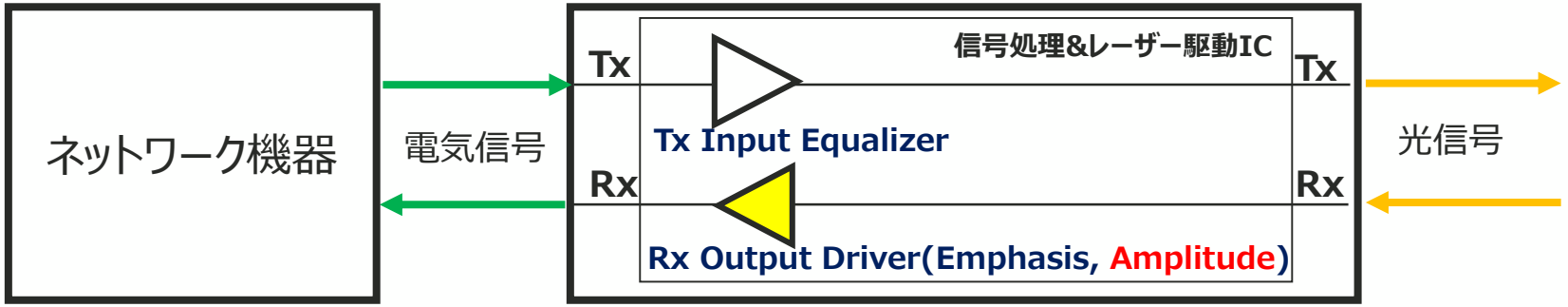


Write/Data	238	0x33	3	Optional Channel Controls	Bit 7-4 = [0011] 600-1200 m(p-p)V Bit 3-0 = [0011] 600-1200 m(p-p)V
Write/Data	239	0x33	3	Optional Channel Controls	Bit 7-4 = [0011] 600-1200 m(p-p)V Bit 3-0 = [0011] 600-1200 m(p-p)V

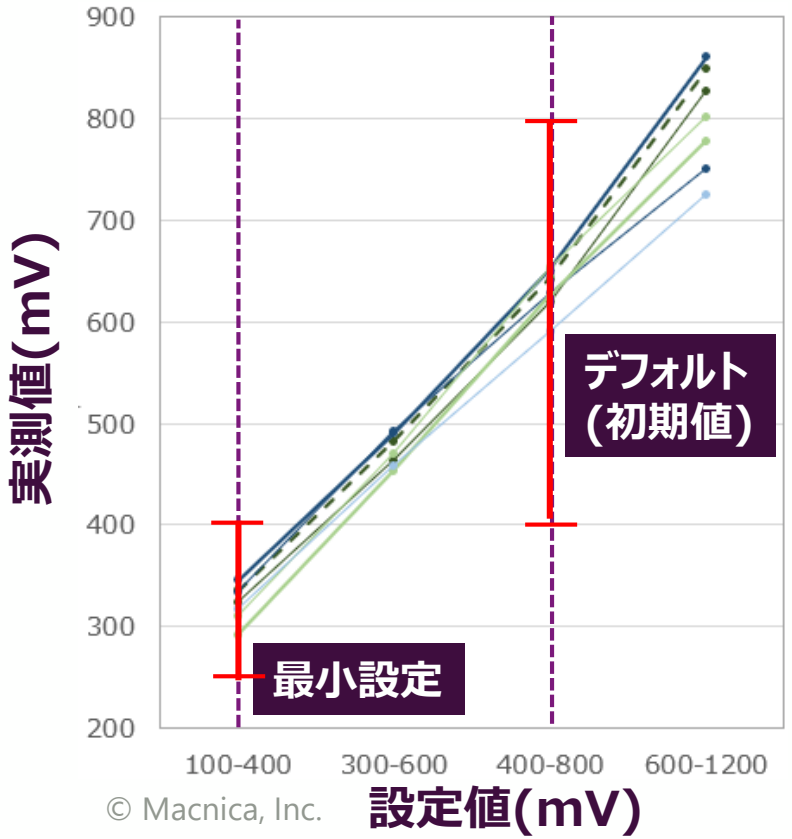
スイッチ内部の基板で信号配線が長い？



ネットワーク装置に渡す電気信号の振幅を最小に設定していたケース



Write/Data	238	0x00	3	Optional Channel Controls	Bit 7-4 = [0000] 100-400 mV(p-p) Bit 3-0 = [0000] 100-400 mV(p-p)
Write/Data	239	0x00	3	Optional Channel Controls	Bit 7-4 = [0000] 100-400 mV(p-p) Bit 3-0 = [0000] 100-400 mV(p-p)



3rd Party Opticsの設定をデフォルトにしたらリンクアップ

まとめ

- 3rd Party Opticsって、選択肢が多く、コストメリットもあります
- 導入時にトラブルが起きると、けっこう解析時間がかかります
- そんなときに役に立つ時短ツールを紹介しました